Investigations on Line-Edge Roughness (LER) and Line-Width Roughness (LWR) in Nanoscale CMOS Technology: Part II–Experimental Results and Impacts on Device Variability

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***Abstract*— In the part I of this paper, the correlation between line-edge roughness (LER) and line-width roughness (LWR) is investigated by theoretical modeling and simulation. In this paper, process-dependence of the correlation between LER and LWR is studied. The experimental results indicate that both Si Fin and nanowire have strongly correlated LER/LWR, and the cross-correlation of two edges depends on the fabrication process. Based on the improved simulation method proposed in the Part I of this paper, the impacts of correlated LER/LWR in the channel of double-gate devices are investigated. The results show that V_{th} distribution strongly relies on cross-correlation, and can exhibit non-Gaussian distribution and/or multipeak distribution, which enlarges the V_{th} variation.**

***Index Terms*— FinFET, line-edge roughness (LER), line-width roughness (LWR), nanowire, variability.**

I. Introduction

SINCE MOSFETs are downscaling into nanometer regime, line-edge roughness (LER) or line-width roughness (LWR) is becoming one of critical issues [1]–[13], especially in multigate devices, where both gate LER/LWR and channel LER/LWR exist. Previous studies usually focus on one subject, namely LER or LWR, and take the results as equivalent. However, there is still difference between the two subjects and neither of them is sufficient for the description of the lateral shape variation of the line alone. It is better to consider LER and LWR as a whole feature, thus, the investigation on the correlation between the two subjects is necessary.

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Part I of this paper [14] introduces a new theoretical model to describe the correlation between LER and LWR, based on the characterization methodology of auto-correlation function (ACF) [3]. The model indicates that LWR ACF has two components: one is LER ACF and the other is LER cross-correlation function (CCF). Additional parameter is proposed to describe the cross-correlation information. In our model, translation length ξ is introduced to reflect the cross-correlation period, while conventional correlation coefficient ρ reflects the amplitude of cross-correlation.

This part shows the experimental research and device simulation results. Fin and nanowire (NW) are fabricated under different formation processes, and then both individual LER property and cross-correlation of the two edges in Fin/NW are investigated. And further simulations are performed to investigate the impacts of correlated LER in double-gate devices.

The rest of the article is organized as follows. In Section II, experimental results are presented, showing strong LER cross-correlation in fabricated Fin/nanowire. Section III is dedicated to device simulation, which indicates the impacts of cross-correlation on device performances. Conclusions are drawn in Section IV.

II. Experimental Results

In order to monitor the characteristics of LER/LWR of multigate devices, Fin channels and NW channels are fabricated, instead of the entire FETs. The process flow followed the process on bulk silicon to approach the realistic fabrication of channels in FinFETs and NW FETs [15], [16]. In order to study the process dependence, the Fin channels are patterned by three different techniques, including hard mask trimming (HT), SiN spacer define (SD), and e-beam lithography (EBL). And nanowire channels are achieved by self-limiting oxidation of the initial silicon bars to get controllable cross-sectional shapes [15]–[21].

LER/LWR can be monitored and extracted from top-view SEM images [3], [6], as shown in Fig. 1. LER ACFs, LER CCF, and LWR ACFs are calculated for each line. We have found that there are three different types of ACFs depending on their shapes, namely, Gaussian type, linear type, and mixed

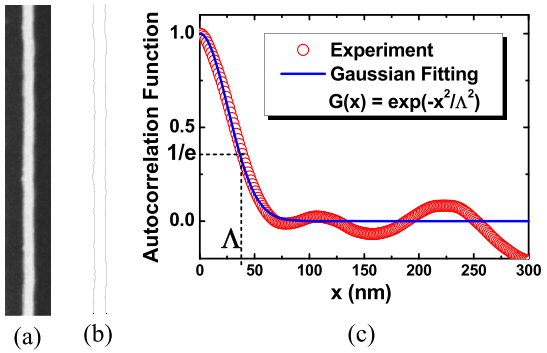

Fig. 1. (a) Top-view SEM image of 40-nm nanowire channel. (b) Edges detected from the SEM image. (c) Auto-correlation function with Gaussian fitting.

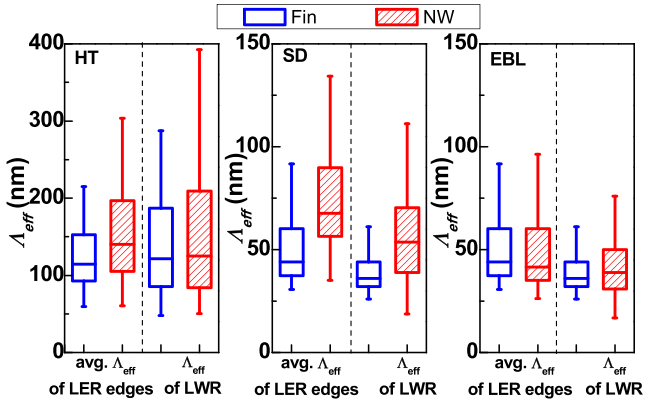

Fig. 2. Box chart of average LER Λ_{eff} and LWR Λ_{eff} of Fin and NW fabricated by three different processes.

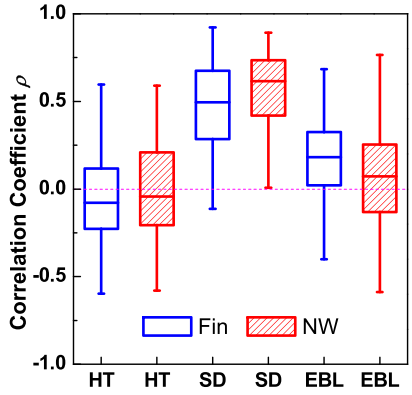

Fig. 3. Box chart of correlation coefficient ρ.

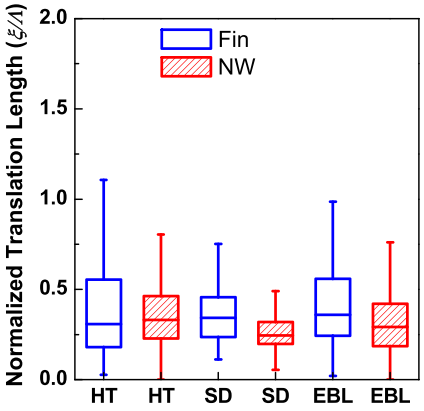

Fig. 4. Box chart of normalized translation length (ξ/Λ_{eff}) of Fin/NW LER by different fabrication processes.

type [6]. LER/LWR with Gaussian-like ACF represents more random variation, while that with linear-like ACF represents more systematic variation. As for mixed type ACF, it can be divided into two parts: Gaussian component and linear component. Δ and Λ of the two parts are extracted individually, then Δ_{eff} and Λ_{eff} are calculated as follows:

$$\Delta_{\text{eff}}^2 = \Delta_G^2 + \Delta_L^2 \tag{1}$$

$$\Lambda_{\text{eff}} = \begin{cases} \Lambda_L & \Delta_G^2/\Delta_{\text{eff}}^2 < e^{-1} \\ \left(\Delta_G^2/\Delta_{\text{eff}}^2\right)\Lambda_G + \left(\Delta_L^2/\Delta_{\text{eff}}^2\right)\Lambda_L & \text{Other} \\ \Lambda_G & \Delta_G^2/\Delta_{\text{eff}}^2 > 1 - e^{-1} \end{cases} \tag{2}$$

where Δ_G and Λ_G represent Δ and Λ of the Gaussian component, respectively; Δ_L and Λ_L represent Δ and Λ of the linear component, respectively.

A. Cross-Correlation of LERs at the Two Edges

Fig. 2 demonstrates the statistics of LER Λ_{eff} and LWR Λ_{eff} of Fin and NW fabricated by different processes. Since Λ_{eff} extracted from the two edges of Fin/NW show symmetric distributions, the average value of two Λ_{eff} from two sides is taken as LER Λ_{eff}. Both the range and median value of NW Λ_{eff} is larger than those of Fin Λ_{eff}, especially under SD technique. This is due to the systematic nature of self-limiting oxidation process, which can smooth the lateral surface by adjusting oxidation velocity depending on the surface condition [16]. Convex surface has the fastest oxidation speed, while concave surface has the smallest one, which means that more silicon is consumed in convex surface than that in concave surface. Thus, the correlation length is enlarged.

Cross-correlation information is also extracted, and Λ_{eff} is used for normalization of translation length ξ. Strong cross-correlation is observed in both Fin LERs and nanowire LERs. On one hand, conventional correlation coefficient has a quite large range, as shown in Fig. 3. HT and EBL patterned Fin/NW LERs have symmetric distributed ρ from negative to positive, while SD patterned Fin/NW LERs mostly have positive correlation coefficients up to 0.9. This is due to the fact that the SD technique is consisted of a conformal deposition process and a highly anisotropic etch process, which guarantee the positive correlation between the two channel edges. But HT and EBL are more like random processes, so those corresponding Fin bars have symmetric correlation coefficient distribution with mean value close to zero.

On the other hand, nonzero translation length is found in most cases, and the value is comparable with correlation length of LER edges, as shown in Fig. 4. Normalized translation length show a less dependency on fabrication process. In most cases, the normalized translation length concentrates between 0.2 and 0.6. However, when compared with correlation

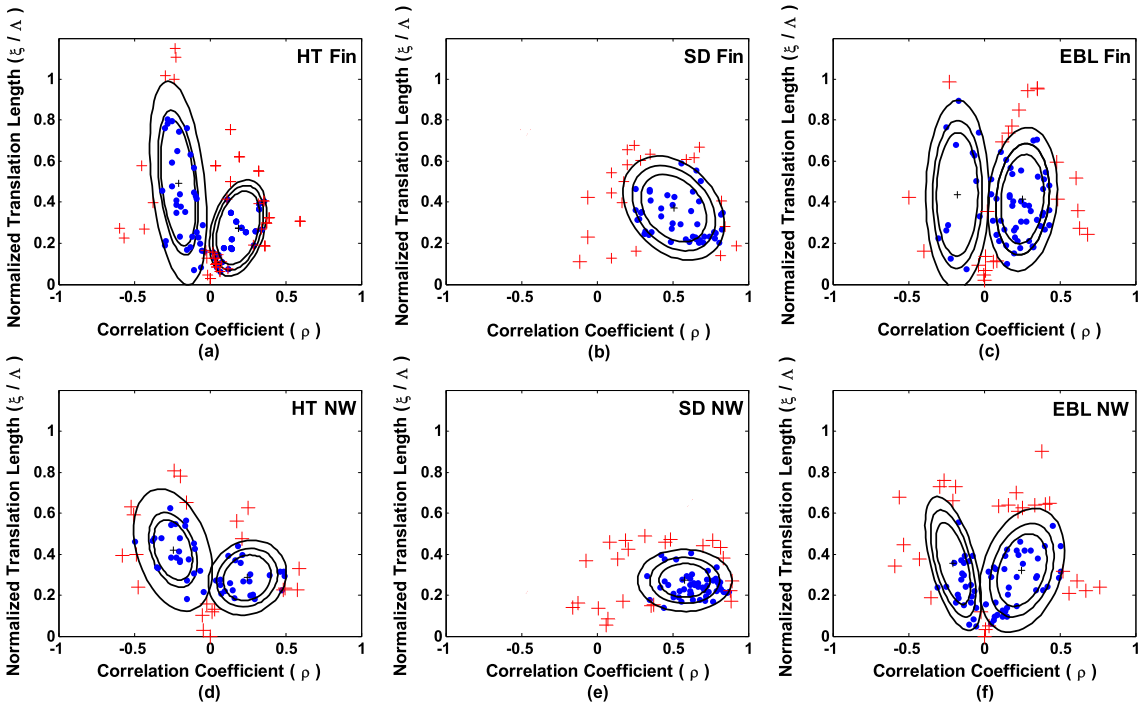

Fig. 5. Normalized translation length (ξ/Λ) versus correlation coefficient ρ extracted from experimental results of Fin/nanowire under different patterning techniques. (a) and (d) HT. (b) and (e) SD. (c) and (f) EBL. Fiducial confidence ellipses are drawn in the picture with confidence level of 0.3, 0.5, and 0.7.

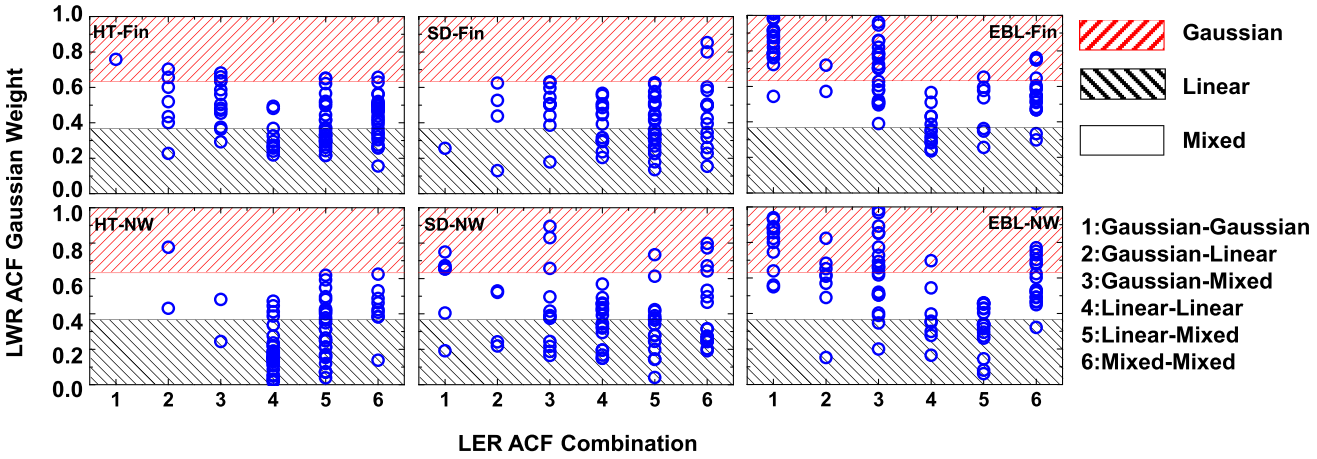

Fig. 6. LWR ACF type versus LER ACF type under different fabrication processes.

coefficient, the process dependency shows up again. The relation between the cross-correlation parameter ρ and ξ is demonstrated in Fig. 5, which indicate that ρ and ξ are not independent. The shapes of confidence region are quite different to each other. In general, more concentrated confidence regions are observed in NW LERs, which means self-limiting oxidation process is helpful to reduce the variation in cross-correlation. In addition, both Fin and NW under HT and EBL techniques show semi-symmetric confidence region when correlation coefficient is negative or positive, while those under SD technique concentrate in the positive correlation area.

B. Correlation Between LER and LWR ACF Types

Previous study shows that there are three different types of ACF depending on the shape of ACF [6]. Part I of this paper has pointed out that LWR ACF type does not rely on the corresponding LER ACF types. Here, it is proved by further experimental results, as indicated in Fig. 6. $\Delta_G^2/\Delta_{\text{eff}}^2$ is defined as weight of the Gaussian component in ACF. And the three types of ACF are defined as follows:

$$\frac{\Delta_G^2}{\Delta_L^2+\Delta_G^2}\begin{cases} < e^{-1} & \longrightarrow \text{Linear} \\ \text{Other} & \longrightarrow \text{Mixed} \\ > 1-e^{-1} & \longrightarrow \text{Gaussian.} \end{cases} \tag{3}$$

All three LWR ACF types can be found under six different LER ACF type combination, which means to determine LWR ACF type, additional information such as cross-correlation between LER edges is needed. Also from Fig. 6, it can be seen that HT and SD techniques lead to more linear and mixed types of LER ACF and LWR ACF, while EBL technique results in

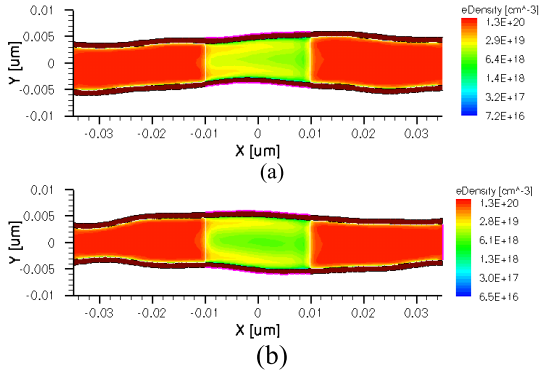

Fig. 7. Electron density distributions of DG devices with $\Lambda = 10$ nm, $\xi = 0$, and (a) $\rho = 0.5$ and (b) $\rho = -0.5$.

TABLE I
CROSS-CORRELATION CLASSIFICATION

Type	ρ	Range of ξ/Λ
(a)	-0.5	0~0.2
(b)	0.5	0~0.2
(c)	-0.5	0.4~0.6
(d)	0.5	0.4~0.6

more Gaussian type LER ACF and LWR ACF. And NW LER and LWR are more linear than Fin LER and LWR under all three fabrication processes, which means the self-limiting oxidation process is helpful to reduce random variation in LER and LWR.

III. IMPACTS ON DEVICE VARIABILITY

In order to understand the impacts of correlated LER on device performance, 2-D statistical simulations with and without consideration of cross-correlation are performed on double-gate (DG) devices with channel LERs. The typical device structure is shown in Fig. 7.

A. Device Simulation

Based on the improved simulation method proposed in the Part I of this paper [14], correlated LER pairs are generated and inputted into Synopsys Sentaurus [22] for device simulation. LER properties of two edges, namely amplitude Δ and auto-correlation length Λ, are set as equal, which fits typical experimental observations. Since the critical dimension of devices shrinking into nanometer regime, it is likely that gate length is going to be smaller than correlation length. Both $\Lambda < L_g$ case and $\Lambda > L_g$ case are considered, namely, Λ is set as 10 or 30 nm.

As mentioned in part I, correlation coefficient reflects the amplitude of cross-correlation, and translation length can be intuitively (yet not rigorously) considered as a reflection of periodic property of cross-correlation. The smaller ρ gets, the weaker cross-correlation is. Correlation coefficient is set as 0.5 or -0.5. Translation length is set in intervals centered in 0 or 0.5Λ. Thus, four typical cross-correlation types are considered in both $\Lambda < L_g$ and $\Lambda > L_g$ cases, as listed in Table I.

TABLE II
SIMULATION SPECIFICATIONS

Parameter	Value
Channel Thickness	8 nm
Oxide Thickness	1 nm
Gate length	20 nm
S/D extension	25 nm
Channel Doping	intrinsic
SDE Doping	1e20 cm^{-3}
LER Δ	0.7 nm
V_{dd}	0.8V

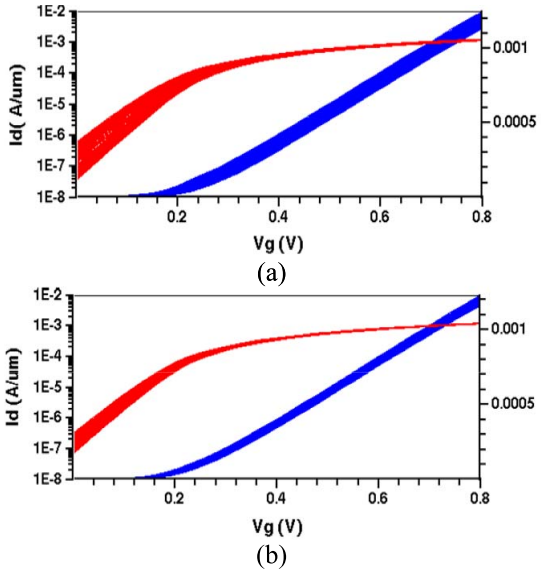

Fig. 8. Transfer characteristics of DG devices with different cross-correlation properties (a) $\rho = -0.5$ and (b) $\rho = 0.5$.

The rest details on the geometry and doping parameters are listed in Table II. For each cross-correlation type, 200 samples are simulated for $\Lambda/L_g = 1.5$, and 500 samples are simulated for $\Lambda/L_g = 0.5$. In addition, 200 samples without consideration of cross-correlation are also simulated for comparison.

In our simulations, the channel doping is intrinsic, so the RDF effect is dramatically reduced. The gate contact is directly added onto gate oxide and WF is set equal, so the WFV effect is also closed. Thus, the variation in V_{th} is mainly caused by LER in the simulations.

B. Results and Discussion

Fig. 8 shows the transfer curves of double-gate devices with different cross-correlation properties, which indicate both cases share similar $\langle I_{on} \rangle$ and $\langle I_{off} \rangle$, but the variation is much larger when ρ is negative. This result is in consistency with previous studies [8]. Negative correlation coefficient means that LER edges are more dissymmetric, leading to larger diameter variation, which has a great impact on device performance variation. The distributions of V_{th} without considering cross-correlation are plotted in Fig. 9. The Quantile–Quantile test (Q–Q test) compared V_{th} distribution with Gaussian distribution by plotting their quantiles against each other. If the shapes of distributions are the same, then the Q–Q plot should

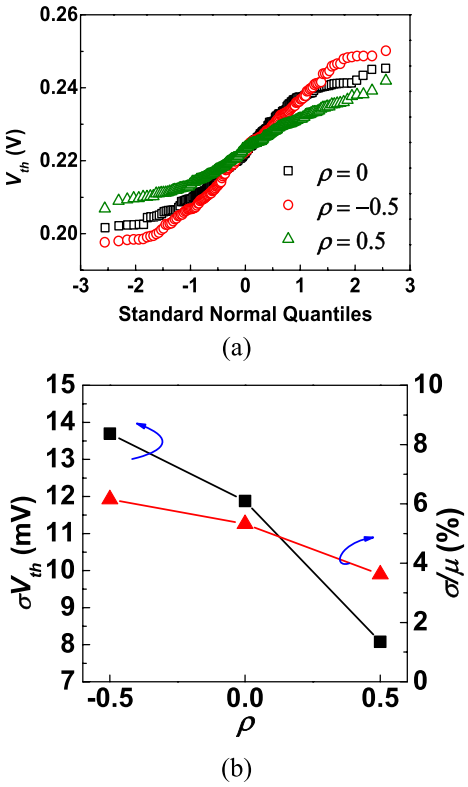

Fig. 9. V_{th} distribution without considering cross-correlation. (a) The Q-Q test shows that conventional V_{th} distributions fit well with Gaussian distribution. (b) Normalized deviation of V_{th} is smaller than 6%.

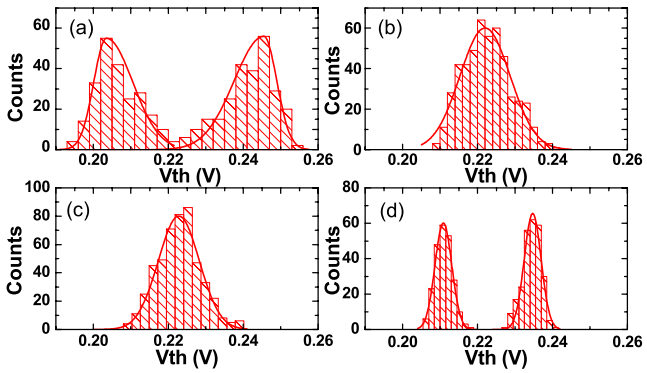

Fig. 10. Distributions of threshold voltage under four types of cross-correlation with $\Lambda/L_{\text{g}} = 0.5$.

be a straight line. Here, we compare V_{th} distribution with the normal distribution. The plot indicates V_{th} distribution from conventional simulation is in consistency with Gaussian distribution, and the variation decreases as the correlation coefficient increases. As indicated in Fig. 9(b), the normalized deviation of V_{th} is smaller than 6%.

However, quite different distributions are found after considering different cross-correlation, as shown in Figs. 10 and 11. This phenomenon is due to the fact that cross-correlation conditions change channel shapes and minimal channel widths, as shown in Fig. 12. When the correlation coefficient is negative and the translation length is zero, the channel edges are more like antisymmetrical [Fig. 12(a) and (b)], leading to double-peak distributed V_{th}. When the translation length

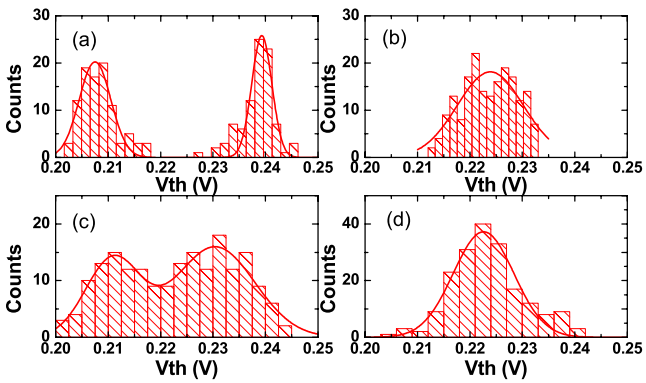

Fig. 11. Distributions of threshold voltage under four types of cross-correlation with $\Lambda/L_g = 1.5$.

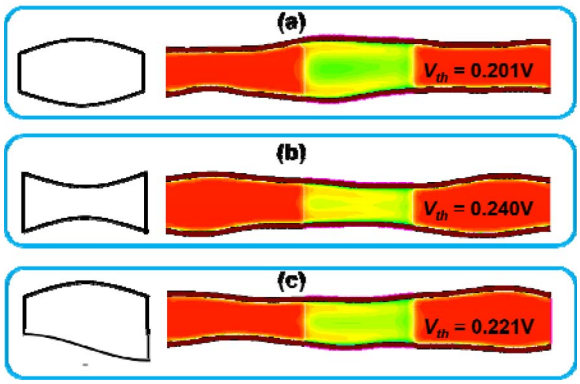

Fig. 12. Explanation for the impacts of cross-correlation condition ($\Lambda = 10$ nm, $\rho = -0.5$). (a) $\xi = 0$, (b) $\xi = 0$, and (c) $\xi = 0.5\ \Lambda$.

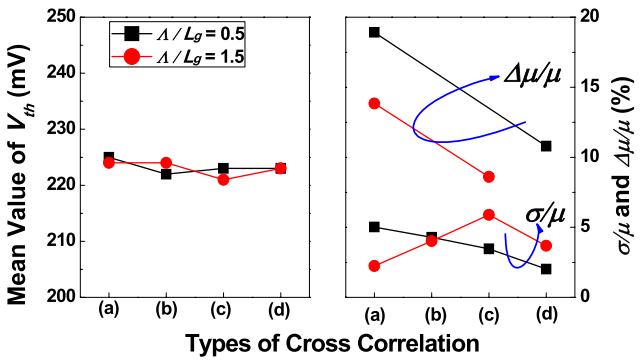

Fig. 13. Four types of cross-correlation share similar mean V_{th} (left); σ/μ is smaller than 10% in four cases while $\Delta\mu/\mu$ is up to 19% (right).

is close to 0.5 Λ [e.g. Fig. 12(c)], the minimal channel width approaches the average Fin width, leading to single-peak distributed V_{th}.

Similarly, if the correlation coefficient is positive and the translation length is zero, the channel edges are more like symmetric, with the channel width equaling the average Fin width. But if the translation length is around 0.5 Λ, channel edges will be close to antisymmetric, leading to double-peak distributed V_{th}.

Non-Gaussian distribution can be observed depending on the cross-correlation type defined in Table I. Thus,

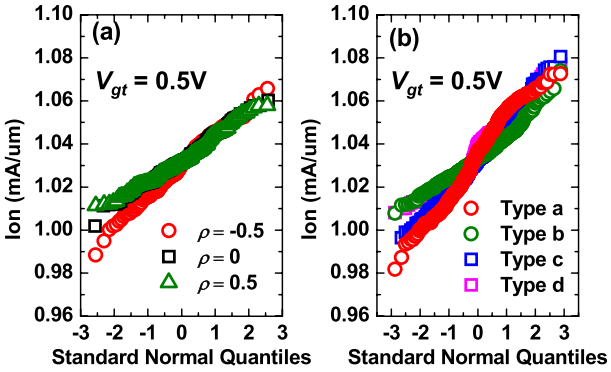

Fig. 14. Q-Q tests of I_{on}. (a) Conventional simulation. (b) After consideration of cross-correlation.

half Gaussian statistics is used for asymmetric distributions [8], [11], in which the standard deviation of the half Gaussian distribution can be evaluated as

$$\sigma = \sqrt{\sigma_L \sigma_R + \left(1 - 2/\pi\right)\left(\sigma_L - \sigma_R\right)^2} \tag{4}$$

where σ_L and σ_R are the standard deviations of left and right parts of the peak.

The total standard deviation of the dual-peak distribution can be evaluated as

$$\sigma = \sqrt{\sigma_1^2 + \sigma_2^2} \tag{5}$$

where σ_1 and σ_2 are the standard deviations of the two peaks.

The resulting statistics are plotted in Fig. 13. The plot indicates that cross-correlation has little influence on the mean value of threshold voltages, since no specific trend is found between different cross-correlation types. However, the impact on variation is quite nonnegligible. Since there are more than one peak found in the distribution, the distance between the peak-centers should also be considered other than traditional standard variation. It is found that $\Delta\mu/\mu$ reaches up to 19% in type (a) when $\Lambda/L_g = 0.5$, three times as conventional normalized standard deviation, which is only 6%. As for the $\Lambda < L_g$ and $\Lambda > L_g$ cases, it can be seen that the appearance of non-Gaussian distribution is a little different, which means that this phenomenon does not simply depends on the cross-correlation type. Other information such as Λ/L_g may also have impact on it. It should be noted that other statistical variation sources such as work function variation can be influenced by LER/LWR, thus, the overall V_{th} distribution may be different from Figs. 9 and 10. Thus, in order to evaluate the impacts of LER/LWR on device performance by simulation, all characterization parameters should be set carefully depending on the fabrication process of interest.

As indicated in Fig. 3, cross-correlation strongly depends on the fabrication process. According to our experimental results in Sec. II, channels patterned by HT technique, are likely to have cross-correlation type (c) and (d) as defined in Table I, those by SD technique are similar to type (b) and (d), while those by EBL are likely to have type (a), (c), and (d).

In addition, variation of I_{ON} is found larger in our simulations than that in conventional one. As shown in Fig. 14, I_{on} is extracted at $V_g - V_{th} = 0.5\,V$ (to decompose the V_{th} caused variation), so the variations of I_{on} can reflect the variation of transport characteristics (e.g., the velocity). According to the simulation results, the impact on I_{on} is not as large as that on V_{th}, as shown in Fig. 14. Whether with or without consideration of cross-correlation, I_{on} exhibits Gaussian distribution. But the deviation in correlated LER cases is a little bit larger than that in conventional cases.

IV. Conclusion

The correlation between LER and LWR is investigated in Part II of this paper by both experiments and simulations. Strong cross-correlation is found between edges in fabricated Fin and NW, and the feature of cross-correlation relies on the fabrication process. And correlation between LER and LWR ACF types discussed in part I of this paper is further confirmed by experimental results, which is that LWR ACF type cannot be entirely determined by LER ACF type without considering cross-correlation. In addition, self-limiting oxidation process is found to be helpful to increase correlation length and reduce Gaussian component in LER/LWR ACF.

The impacts of correlated LER are studied by simulations based on double gate devices. The results indicate that V_{th} distribution has strong dependence on the cross-correlation between LER edges, which was missing in previous studies. Non-Gaussian distribution is observed, which shows a much larger variation than that in conventional simulation. As a result, the LER effect could be under-estimated if the cross-correlation of LERs is not taken into account.

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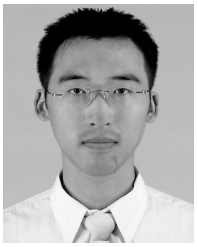

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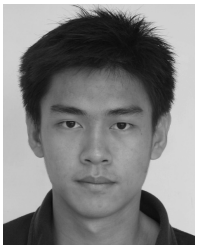

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