Journal of
Micro/Nanolithography,
MEMS, and MOEMS

Nanolithography.SPIEDigitalLibrary.org

Self-aligned double-patterning layout decomposition for two-dimensional random metals for sub-10-nm node design

Yongchan Ban
David Z. Pan

SPIE.

Self-aligned double-patterning layout decomposition for two-dimensional random metals for sub-10-nm node design

Yongchan Ban[a,*] **and David Z. Pan**[b]
[a]System IC R&D Lab., LG Electronics, Seoul 137-893, Republic of Korea
[b]University of Texas, Department of Electrical and Computer Engineering, Austin, Texas 78712, United States

Abstract. Self-aligned double patterning (SADP) is popularly in production use for one-dimensional-type dense patterns with good pitch control in NAND Flash memory applications and the fin layer patterning of FinFET devices, but it is still challenging to apply SADP to two-dimensional (2-D) random metal patterns. We describe the SADP layout decomposition methods for complex 2-D layouts. The SADP for complex logic metals consists of a two mask approach using a core (mandrel) mask and a trim mask. This paper describes methods for automatically choosing and optimizing the manufacturability of base core mask patterns, generating assist core patterns, and optimizing trim mask patterns to accomplish high quality layout decomposition in the SADP process. Our technique is validated with 22-nm node industrial standard cells and logic designs, which can be applicable to sub-10-nm node design. Experimental results show that our proposed layout decomposition for SADP effectively decomposes many challenging 2-D layouts. [DOI: 10.1117/1.JMM.14.1.011004]

Keywords: self-aligned double patterning; decomposition; lithography; two-dimensional random metals; 10-nm node; layout design.

Paper 14105SSP received Jul. 3, 2014; revised manuscript received Sep. 6, 2014; accepted for publication Oct. 13, 2014; published online Dec. 4, 2014.

1 Introduction

Since a 193-nm wavelength light source is still used for printing sub-40-nm half-pitch patterns, current state-of-art lithography has reached the fundamental limitations.[1–3] Next-generation lithography (NGL) techniques, such as extreme ultraviolet, e-beam direct write, etc., are introduced to achieve high resolution patterning. However, there are still several hurdles to face, i.e., high cost, difficulty of materials and processes, or low throughput.[1,4] To bridge the gap between ArF (193-nm wavelength) lithography and NGL technologies, double-patterning technology (DPT) with traditional ArF lithography tools has been a promising alternative to achieve high resolution for sub-30-nm nodes.[5,6] The main idea of DPT is to decompose a single layout into two masks in order to increase the pitch size of each mask and improve the process tolerances of focus and dose variations.[4,7–9]

DPT largely consists of two types: a litho-etch-litho-etch (LELE) double patterning and a spacer type self-aligned double patterning (SADP). LELE has two lithography steps with one or multiple etch steps.[1,8–11] The basic idea of LELE is to decompose one mask layout into two mask layouts where the pitch of each mask layout pattern should be doubled. Thus, a step of a bipartite layout coloring is crucial, and any odd cycle of the layout polygon in the target design should be removed. If some polygons should happen to meet an odd cycle, one of the polygons should be split into two or more polygons to resolve the layout decomposition conflicts, which will introduce "stitch" points as shown in Fig. 1.

The critical limitation of LELE is the inevitable overlay error between the two sequential exposure steps. The mask placement, alignment, and magnification errors on the second mask exposure might induce patterning variation, which directly causes significant performance and yield degradation.[12–14] In addition, a stitch can be regarded as though it acts like a line-end which is highly sensitive to lithography process variation and is prone to line-end shortening, critical dimension (CD) shrinking, etc.[1,8,15] Moreover, since the second images are exposed on top of the first generated patterns with a nonplaner substrate topography, wafer topographic effects, such as shadowing and nonuniform reflectivity, may cause considerable patterning variation on the final wafer images.[15–17]

Since SADP has fewer overlay requirements and excellent variability control compared to LELE DPT, it has been getting more attention for sub-20-nm node device patterning. SADP is a pitch-splitting sidewall image method that also utilizes two masks: a "core" mask and a "trim" mask. The core mask defines the core mandrel patterns, and the sidewall spacer is deposited onto all sides of a mandrel pattern to enable pitch doubling in the patterning. The trim mask removes unnecessary patterns by blocking or unblocking with photoresists (PR). Since the most critical patterning control in SADP is not governed by lithography but by the deposition of the sidewall spacer, it has less overlay error and excellent variability control compared with LELE.[14,18–20]

However, SADP allows only a single width of sidewall spacer which forms either a single-wire width or a

*Address all correspondence to: Yongchan Ban, E-mail: yc.ban@lge.com

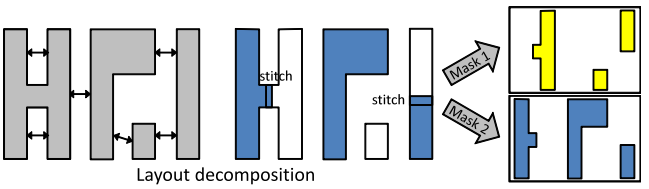

Fig. 1 Litho-etch-litho-etch (LELE)-type conventional double-patterning technology: it is very sensitive to the mask overlay error and the process variation.

single-wire space. Therefore, SADP was previously limited by the lack of flexibility in terms of layout decomposition. Thus, SADP is only in production use for one-dimensional patterns in NAND Flash memory applications, but applying SADP to two-dimensional (2-D) random logic patterns is challenging.[18,21,22] Due to its limitation, SADP might require three masks for a 2-D-type application. Since the manufacturing cost of logic products is dominated by the patterning cost (the number of masks), a two-mask SADP approach is necessary for successful product application. Thus, layout decomposition for random 2-D logic features which have various wire widths and spaces is a primary challenging issue for a manufacturable SADP process.

In this paper, we propose rigorous layout decomposition methods for the SADP technique for sub-10-nm node random shaped metal layouts. This paper describes several SADP-aware layout coloring algorithms and a method of generating lithography friendly core mask patterns. The major contributions of this paper include the following:

- This paper develops a systematic framework SADP layout decomposition for 2-D layout structures, where two masks (the core mask and the trim mask) are used. Base core mask patterns are made up of "main core patterns," which are chosen from the original layout using our SADP-aware layout coloring and "assist core patterns," which can be generated in a lithography friendly manner.
- The layout coloring is a crucial step in SADP decomposition. Despite not using any stitches, we can resolve coloring conflicts with the proposed approaches. The layout coloring highly affects the manufacturability of the core mask and trim mask layout. To resolve manufacturing conflicts on the core mask layout, we propose a grouping and merging algorithm. Meanwhile, we propose a trim mask friendly coloring incorporated with shortest-path coloring, which can produce the best coloring layout for the trim mask layout.
- We evaluate our technique on 22-nm node industrial standard cells and static random access memory (SRAM) logic designs which can be applicable to sub-10-nm node designs. By introducing layout retargeting, we can achieve a feasible SADP decomposition for random 2-D designs which shows various spaces and widths.

The rest of the paper is organized as follows. Section 2 describes SADP lithography processes and the challenging issues. Section 3 presents several layout coloring approaches for design rule check (DRC)-free decomposed mast layouts. Section 4 proposes algorithms of the core mask generation. A type of SADP compliant layout is presented in Sec. 5. Experimental results are discussed in Sec. 6, followed by conclusions in Sec. 7.

2 Spacer-Type Double Patterning

We first introduce some terminologies and notations which are used throughout this paper:

- Core mask: the first mask in the SADP process flow.
- Mandrel ($M_\forall$): the printed patterns generated by the core mask where the sidewall spacers are subsequently formed. It is often used as a synonym for core mask layouts. A mandrel consists of a main mandrel and an assist mandrel.
- Main mandrel (M_m): the base mandrel (core mask) layout which is a chosen subset of the original design intent.
- Assist mandrel (M_a): the extra mandrel layout newly generated, i.e., assist features, to make patterns (secondary patterns) by forming sidewall spacers near the assist mandrel.
- Secondary (≡2ndary) pattern (P_s): the pattern except for the main mandrel in the original layout. It is eventually generated by merging sidewall spacer patterns near mandrel layouts.
- Spacer (S_p): the sidewall spacer, which is deposited on the mandrel layout, is formed at both sides of the mandrels.
- Trim mask (T_m): the second mask in the SADP process flow, which is used for removing unnecessary patterns.

Two types of SADP process are popularly used for the state-of-the-art lithography patterning: SIM-type SADP and SID-type SADP. Figure 2 shows the vertical view of SADP process sequences for SIM (a) and SID (b) type SADP. SIM is an abbreviation of "spacer is metal," where the sidewall spacer itself becomes the final metal pattern. Core layout, which is called the mandrel layout and becomes the first mask layout in SADP, is designed based on the space region between the metal lines as in Fig. 2(a)-(2). Then, the side-wall spacers are generated based on the core mandrel layout in Fig. 2(a)-(3). After removing mandrels in Fig. 2(a)-(4) and processing the second mask trimming step in Fig. 2(a)-(5), the final dense features are patterned on the wafer matched with the design intent in Fig. 2(a)-(6).

The other type of SADP is SID which is an acronym for "spacer is dielectric." The steps are similar to SIM, but in SID-type SADP the side-wall spacer is just dielectric. Meanwhile, the mandrel layout becomes the final metal pattern. The base mandrel layout is chosen from the original layout as shown in Fig. 2(b)-(2). Then the sidewall spacers are generated near the mandrel layout in Fig. 2(b)-(3). After removing the mandrels, we deposit substrate materials in Figs. 2(b)-(4). Then the second trimming mask is used for getting the final patterns in Fig. 2(b)-(5) and 2(b)-(6). Since the base mandrel layout is a subset of the original layout and should have enough layout pitch for the first lithography patterning, it is usually chosen from the layout coloring.[14,18]

Since the width of the sidewall spacer is constant, it is hard to vary the pattern line-width in an SIM-type SADP

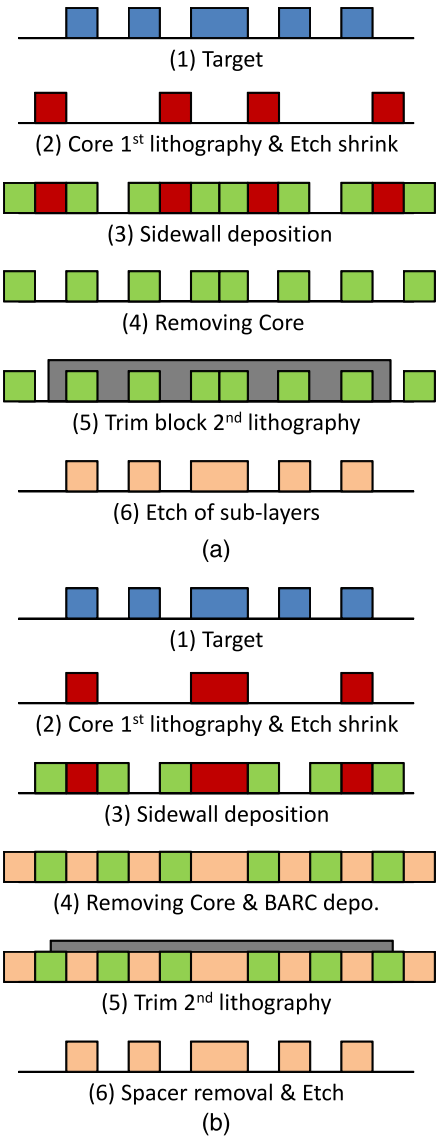

Fig. 2 Two types of self-aligned double pattering: (a) SID-type self-aligned double patterning (SADP) enables various metal widths and has fewer process steps than (b) SIM-type SADP.

because the sidewall spacer becomes the metal line. In SID-type SADP, however, it is hard to control the pattern space because the side wall spacer becomes a space between two mandrel metal patterns in SID. Since the core mandrel layout in the SID-type SADP becomes the final metal pattern, the SID-type SADP enables various metal widths. Moreover, as the SID-type SADP has fewer process steps than the SIM-type SADP, it provides more cost effective metal patterning.[18,23] Thus, we focus on the layout decomposition of the SID-type SADP in this paper. However, our methodology is not limited to SID-type SADP decomposition but is also applicable to SIM-type SADP by simply modifying the input conventions.

Let us look at SID-type SADP sequences from a top view in Fig. 3. The layout coloring is first done to select the base mandrel from the original target in Fig. 3(2). Either color between two colored layouts can be the base mandrel in our approach. Then, extra mandrel layouts (assist mandrel) are added on the base mandrel to eventually make patterns, which are not chosen for the base mandrel in Fig. 3(3). Note that the first core mask is usually biased and bigger than the design intent for better lithography printability in Fig. 3(3). After decreasing the first mandrel pattern as much as the target size in Fig. 3(4), the sidewall spacers are formed around the mandrel as in Fig. 3(5). After removing the mandrels in Fig. 3(6) and depositing the substrate material, e.g., bottom anti-reflection coating (BARC) in Fig. 3(7), we remove the unnecessary polygons except for the design intent with the trim mask in Fig. 3(8), where a secondary pattern is formed.

One can see an assist mandrel layout which is added on the main mandrel and will not be printed on the wafer to eventually make the secondary pattern ("not mandrel") using a trim mask. By applying layout coloring, one color can become the main mandrel. The selection of the main mandrel color affects the shapes of the assist mandrel layouts. In a random 2-D layout application, inserting assist mandrel polygons is an essential part because those allow various wire widths and various pattern shapes in the SADP layout decomposition. Therefore, one can make random 2-D shape patterns by building assist mandrel layouts.

However, a major drawback of the SADP is the fact that features in SADP do not allow any stitch points as in LELE. This means that splitting a polygon into two or more polygons cannot be allowed in SADP. Thus, one polygon should have one particular color. This is because the selected mandrel will make sidewall spacer patterns near the mandrels, and in case one polygon has a stitch point (decomposes into two polygons) such as in LELE, there is no way to connect two different colored layouts. The spacer acts like a layout separator between the main mandrels and the secondary patterns. Stitch insertion would result in disconnecting the final patterning results due to spacer blocks.

Even though stitching can have side effects such as yield loss due to mask overlay, a stitch insertion gives a decomposition flexibility to LELE. Without stitch insertion, some coloring conflict is usual in a random 2-D layout. Figure 4 shows some cases of coloring conflict. By inserting a stitch point in LELE DPT, the coloring conflict can be resolved as in Fig. 4(1). Not all the conflicts can be resolved by inserting stitches, however, even in LELE. The undecomposable conflict in Fig. 4(2) is called an inherent or native conflict.[1,24] Since SADP does not allow any stitch insertion, both (1) and (2) in Fig. 4 can be regarded as native conflict cases. Therefore, resolving coloring conflicts is another critical step in the SID SADP process for random 2-D layouts.

There are many challenges involved with creating a core mandrel mask and a trim mask for complex 2-D layouts. In particular, the layout coloring and assist mandrel generation are important steps in an SADP mask synthesis process:

Layout coloring. Since the main mandrel is chosen from the design intent after assigning a color mapping, the manufacturability on both core mask and trim mask is significantly dependant on layout coloring. A core mask layout can be easily generated from the main mandrel, yet the trim mask layout is relatively less intuitive. Moreover, since SADP does not allow any stitch insertion, it is crucial to resolve any odd-cycle coloring conflicts in the SADP layout decomposition.

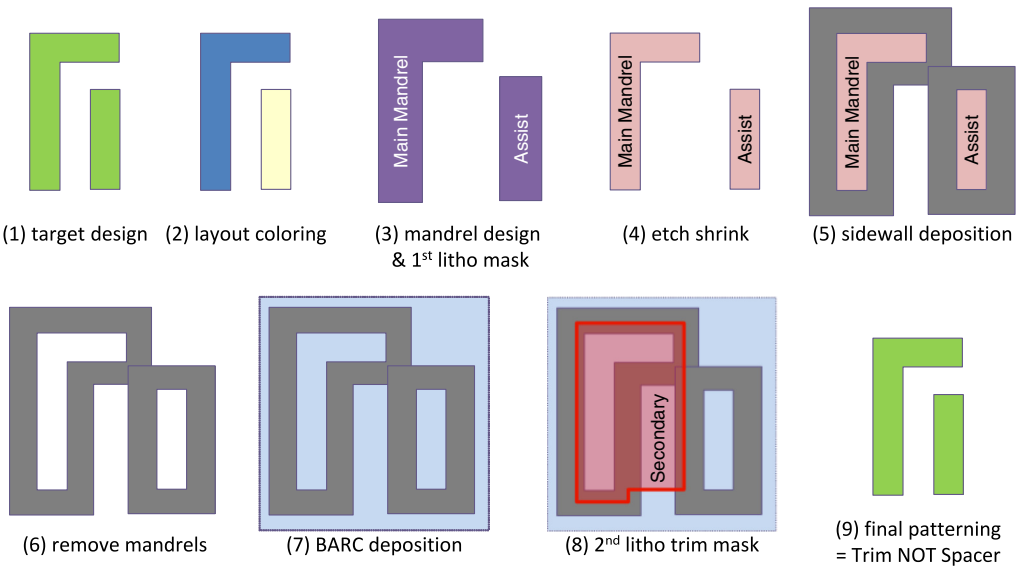

Fig. 3 The top view of SID-type SADP process: the patterning control is governed by the deposition of the sidewall spacer.

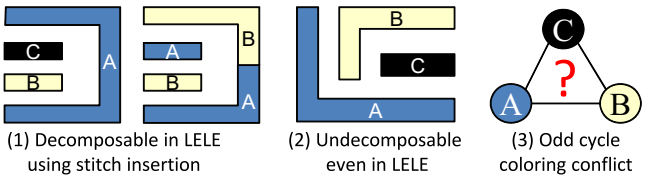

Fig. 4 Coloring conflicts in layout decomposition in LELE double patterning.

Assist mandrel. Assist mandrel gives SADP more flexibility which allows us to make a randomly shaped layout. Thus, it requires intelligently designed mandrel layouts as a good starting point. Since the first core mask is usually more complex than the trim mask, it highly affects lithographic printability on the wafer. Thus, a lithographic friendly mandrel generation is necessary for less process variation.

3 SADP Aware Layout Coloring

3.1 *Problem Formulation*

Given: In a given layout L, let $F = \{f_i | 1 \le i \le n\}$ be a set of polygon features and $E = \{e_j | 1 \le j \le m\}$ be a set of edge segments in a feature f_i, and d be the minimum coloring distance between two polygon features. **Find**: To minimize the sum of connections among the polygons on a layout. **Subject to**: (1) A connection weight in a feature f_i is the sum of the assigned weights of all edges e_j, (2) A positive connection between two polygons encourages placement on the opposite color. (3) A negative weight encourages placement on the same color.

Even in a polygon, every branch of a polygon might have a different neighboring layout connection. A conventional layout coloring regards one polygon as one node regardless of the length or neighboring conflict of the polygons. However, each polygon has a different priority. Thus, the decision of the main mandrel from the colored polygon is crucial in SADP layout decomposition. We propose an edge segment-based layout coloring. By calculating the connection weight on edge segments instead of on every polygon node,[1,9,24] we can consider the layout connection constraint. The reasons why we use an edge segment–based coloring are as follows:

- SADP mask decomposition does not allow "stitch" points. Every polygon should have a single color without division. Thus, we should more accurately calculate connection weights in a layout. Edge segments can consider every local layout constraint for SADP mask decomposition.
- In SID-type SADP, the first core mask layout is decided from target polygons, meanwhile the shape of the second trim mask layout is highly related to layout spaces between two polygons (refer to the Sec. 3.2). Edge segments of polygons provide better layout information for the trim mask.

Figure 5 shows a color assignment based on an edge segment approach. The first step is to divide every edge of the polygons into multiple segments based on the polygon itself and neighboring polygons, which is similar to the layout segment of a conventional model-based optical proximity correction (OPC). Then, each edge in a polygon calculates the connection weight. For example, in Fig. 5, the distance between an edge e_4 of a feature f_1 and an edge e_{31} of a feature f_2 is less than the minimum coloring distance d. Thus, the edges e_4 and e_{31} have positive weight. Whereas, since the space of an edge e_3 of a feature f_1 is larger than d, no weight value is given. The connection weight of a polygon can be the sum of the connection weights of all edges.

Our overall layout coloring for an SID-type SADP is given in Algorithm 1.

3.2 *Grouping and Merging Coloring*

Since SADP mask decomposition does not allow stitch insertion, some coloring conflict is usual. As shown in Fig. 6, the target design has a native coloring conflict which represents

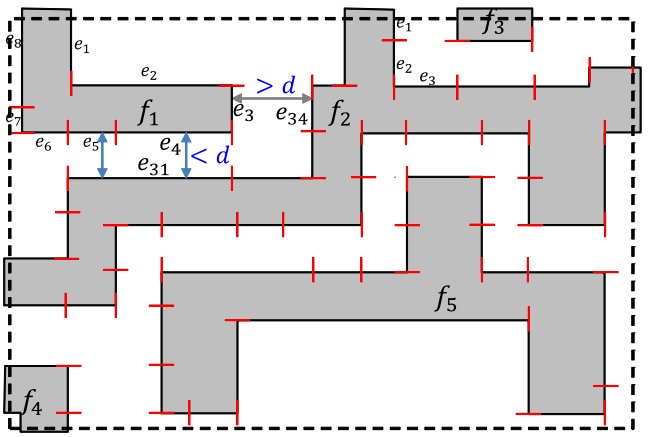

Fig. 5 Edge segment-based layout coloring: when coloring a layout, we consider connection weight on edge segments.

an undecomposable layout even in LELE.[9,24] To resolve this coloring conflict, we introduce a grouping and merging algorithm. Once two same colored polygons are within the minimum coloring distance d, we make a group for the polygons and merge them into one polygon. By merging

Algorithm 1 Mask aware layout coloring.

1: Dummy layer insertion in Sec. 3.5

2: A set of polygon features F in a layer

3: Find self-conflict areas in Sec. 3.4

4: A set of self-conflict areas S in a layer

5: **for** each polygon $f \in F$ **do**

6: $\text{Weight}_f \leftarrow 0$

7: Decompose segments $E \in f$

8: **for** each segment $e \in E$ *do*

9: $\text{weight}_e \leftarrow 0$

10: detect conflict c with min. distance d

11: **if** $c < d$ **then**

12: determine whether conflicted layout $\in S$ or not

13: update weight_e, shortest-path coloring in Sec. 3.3

14: **end if**

15: $\text{Weight}_f += \text{weight}_e$

16: **end for**

17: **end for**

18: assign a color for polygons with a sparse matrix solver

19: check grouping in Sec. 3.2

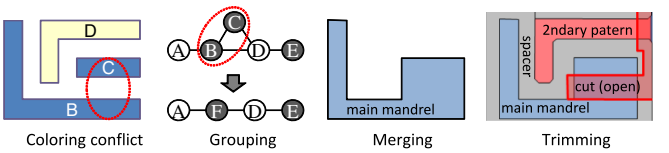

Fig. 6 Grouping and merging coloring: we propose a grouping and merging algorithm to resolve coloring conflicts.

the two conflicted polygons, we can make a core mask without any DRC and lithography violation. This merged region between two grouped polygons should be trimmed out at the second trim mask patterning step. In this step, even though the space between polygon B and polygon C would be small ($\simeq$minimum space), the cut mask patterning at the second trim mask should be good because it is an isolated pattern with a huge pitch.

Note that since the spacer patterns of nearby mandrels will become dielectric (nonmetal patterning area) after the trim mask patterning, the spacer acts like an overlay-free region. It implies that if the edge of a trim mask layout is on the spacer region, the trim layout can be free from mask overlay variations without any impact on target metal lines. In the other words, we should carefully control the mask overlay if the trim mask edge is on metal lines.

Thus, we should note the following issues if a trim mask should cut the merged area:

- The width of a trim mask should meet the trim mask width constraint, which is usually the same as the minimum target layout width or slightly larger.
- Since the edge of a trim mask layout is passing over the main mandrel and not the safe spacer region, the overlay error of the trim mask should be carefully controlled.

3.3 *Shortest-Path Coloring*

After merging two conflicted polygons into one polygon, the trim mask should remove the merged region at the cost of mask overlay. Therefore, a shorter trim mask for removing a merged region is preferable for its smaller overlay impact on the Second patterning. Therefore, in addition to a grouping and merge coloring, we propose a shortest-path coloring as shown in Fig. 7. The shortest-path coloring is achieved by reflecting the length of an edge segment when we assign a

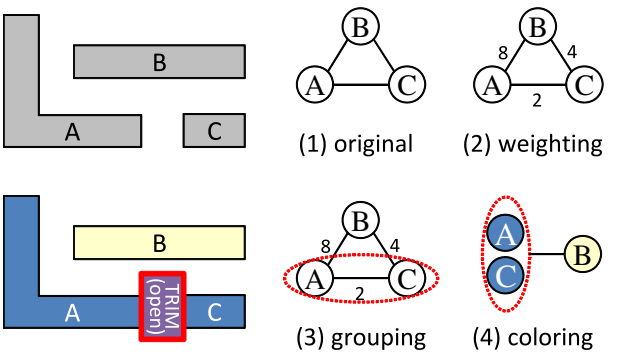

Fig. 7 Shortest-path coloring: a shorter trim mask for removing merged region is preferable for a smaller overlay impact.

connection weight on an edge. In Fig. 7, the region between polygon A and B has a longer interacting length of coloring conflict. Meanwhile, the region between polygons A and C has the shortest interacting length. The interacting length is multiplied by the interacting weight for both polygons. Thus, the polygons having a smaller interacting length have a lower interacting weight for coloring that makes the shortest interacting polygons have the same color.

3.4 *Self-Conflict Aware Coloring*

Even though we assign the same color on the polygons which have less polygon interference, the corresponding trim mask might have internal DRC errors on the mask itself because the trim mask should meet single-patterning constraints as shown in Fig. 8. In order to avoid this self-conflict violation, we identify self-conflict regions of the trim mask and put more interacting weight in layout coloring. The self-conflict region on a trim mask usually happens when three or more consecutive polygons have the same color where the width of the middle polygon is less than the trim mask space constraint. We can detect the trim self-conflict region by twice checking the minimum space of the layout. The min. space check is shown in Fig. 9. By putting more connecting weight on the self-conflict region, we can avoid the internal DRC error on the trim mask.

3.5 *Trim Mask Friendly Coloring*

Since the sidewall spacer can be placed between two abutting metal polygons, it can exactly identify the edge position of different metal lines. It implies that the sidewall spacer prevents abutting metal lines from patterning faults, in particular, a bridging fault. Moreover, it can give the trim mask more process tolerance. As shown in Fig. 10, a conventional layout coloring might give a smaller patterning margin, e.g., narrower trim width or width violation. In addition, the trim mask is prone to mask overlay. The best possible coloring for an SID-type SADP is to assign a different color to polygons in every other layout pitch track.

To assign the best coloring on the layout, we insert dummy layouts between two metal lines as shown in Fig. 11. Once we put dummy metals into vacant areas, we assign the two-map layout color with the shortest-path coloring and the self-conflict aware coloring approaches. After removing the dummy metals, we can get the trim mask friendly layout coloring for the SID-type SADP process.

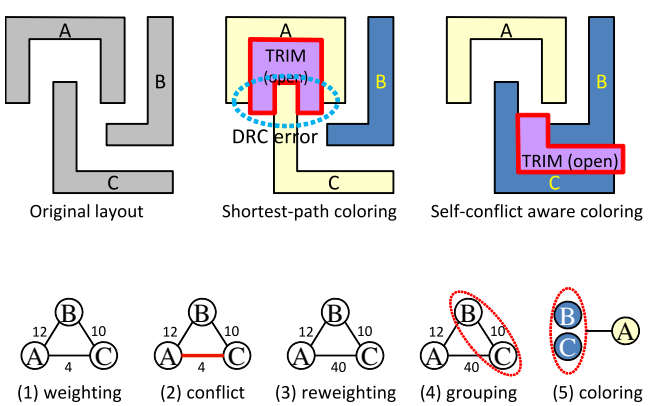

Fig. 8 Self-conflict aware layout coloring: when three or more consecutive polygons have the same color, the self-conflict region on a trim mask could happen.

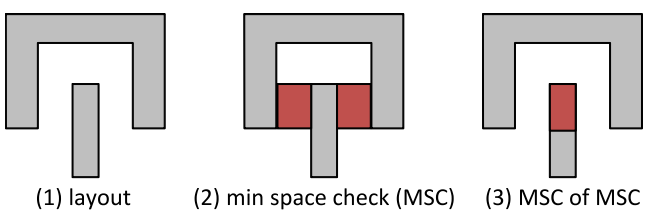

Fig. 9 Define the self-conflict area: we can detect the trim self-conflict region by checking the minimum space of the layout twice.

4 Lithography Friendly Mandrel Generation

4.1 *Problem Formulation*

Given: Let M_m be the main mandrel, P_s be the secondary patterns, L_m be the minimum mandrel width at the wafer, L_s be the minimum spacer width at the wafer, and L_b be the mask bias for the first patterning. **Find:** Find the assist mandrel, M_a, to make secondary patterns, P_s, at the final patterning by merging the sidewall spacer patterns, S_p near the core mandrel, $M_\forall$. **Subject to:** (1) no DRC error is allowed between positively biased (increased) $M_\forall$ (M_m and M_a) to be as much as L_b on the first core mask. (2) DRC error is allowed between M_as itself because M_a will be removed at the second trim mask step.

Figure 12 illustrates a way to generate assist mandrel patterns in addition to the main mandrel. The goal of the assist mandrel, M_a, is to make secondary patterns, P_s, by merging neighboring spacers S_p of the nearby Mandrel, $M_\forall$. There should be spacer patterns next to every secondary metal P_s. Since $M_\forall$ makes S_p which also generates P_s in an intuitive way, we can make M_a in every neighboring P_s as much as L_s. Meanwhile as M_m also generates S_p patterns, we can filter out overlapped M_a which lie on the interacting region of M_m within the distance $(L_s + 2L_b)$.

Algorithm 2 also shows a flow of our mandrel generation for a 2-D random layout. The assist mandrel is formed using polygon extension and Boolean operation of polygons in line 2 to 10. After making additional mandrel patterns, we cut some overlapped region with the main mandrel in lines 11 to 13. Once some small jogs and spaces in the additional mandrel are modified with a manner that is manufacturing friendly in lines 14 to 18, we adjust the final metal pattern with a metal retargeting rule in line 19.

4.2 *Lithography Friendly Assist Mandrel*

Figure 13 shows the final core mask layout $(M_m + M_a)$ in different ways. We can generate assist mandrel patterns for 2-D random layouts with different options, for example the shorter the M_a, the longer M_a and the directional M_a. The shorter M_a approach builds M_a polygons just at the area facing with the secondary metal, P_s. This approach induces lots of small island patterns. Some small patterns in the core mask are prone to collapse due to PR tension or to be moved away due to lithography proximity. Thus, one can also use the longer M_a approach which generates M_a patterns covering all the surrounding areas of P_s.

Another option is the directional M_a approach which makes M_a by considering lithography illumination.

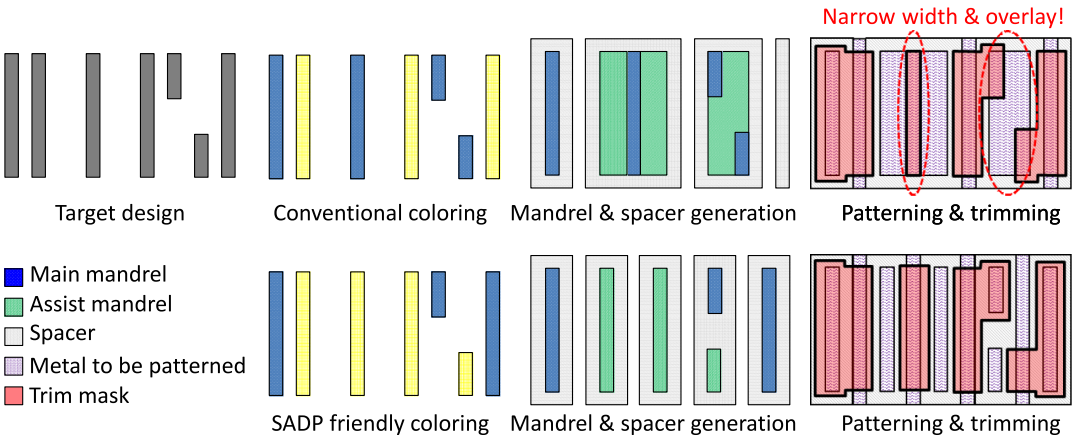

Fig. 10 Trim mask friendly coloring: the best coloring for SID-type SADP is to assign a different color on polygons in every other layout pitch track.

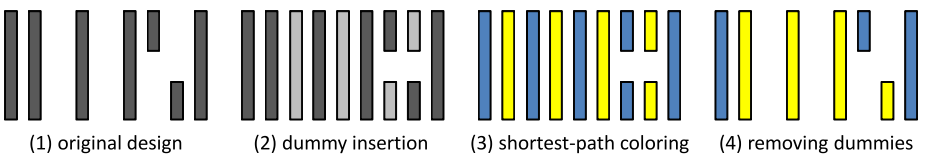

Fig. 11 Dummy insertion for trim friendly coloring: we can get better coloring result for SADP layout decomposition.

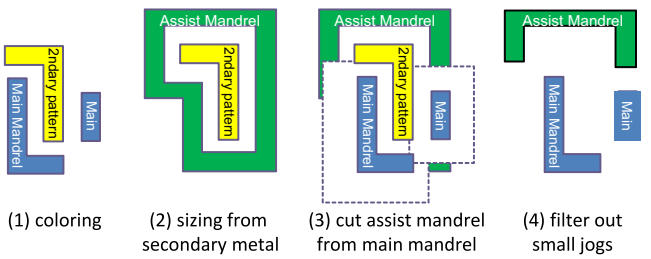

Fig. 12 Generation of assist mandrel: the goal of the assist mandrel is to make secondary patterns by merging the neighboring spacer of nearby Mandrel.

Off-axis illumination is widely used for better lithographic printability. An oblique illumination improves the patterning resolution of those features toward the illumination direction.[25] It directly implies that a single-directional metal layout is desirable for lithography patterning. Thus, in the directional M_a approach, we generate M_a at the area which has the same direction as the metal lines. This approach is similar to the shorter M_a approach at the first stage, yet by removing a small island, which is usually located at the metal line-end, we can achieve directional M_a polygons.

4.3 *Assist Mandrel Postprocessing*

If the space among M_as is smaller than a certain constraint, we can fill a space and make a polygon by connecting M_as in order to not violate the mask rule in the core mask. Once we connect between two M_as, the corresponding P_s might be also connected. Thus, the connected region at P_s should be removed at the second trim mask step [Fig. 14(a)]. Note that the smaller space at the trim mask would be no problem because it is an isolated space having a huge pitch size. If a space or a width guarantees a high enough pitch, the patterning would be good for applying advanced OPC and retargeting.

In a similar way, if small pieces of M_a are in conflict with M_m, we can merge them into M_m or remove them. When small M_a is merged into M_m, both the merge area and the small M_a should be cut at the trim mask, which might be an overlay burden to M_m. Meanwhile, when the small M_a is removed, the P_s region might be extended, it should be removed, which might give an overlay burden to P_s [Fig. 14(b)]. If a piece of M_a is smaller than a certain constraint, we can remove it [Fig. 14(c)].

5 Study of SADP Compliant Layouts

5.1 *SADP Compliant Layouts*

A random metal layer has various shapes of layouts. When decomposing a 2-D layout, we happen to meet a lot of DRC conflict on both the core mask and trim mask. Thus by studying several cases of layouts which seem to be hard to decompose, we can have more flexibility for SADP layout decomposition, SADP-aware routing, and so on.

5.1.1 *Line-end control*

According to a previous research,[18] the minimal space between two line-ends (tip-to-tip) in LELE DPT is twice as much as that of SADP. This is mainly because the tip-to-tip space can be achieved by the cutting (trim) mask. Thus, the minimal space in SADP is highly dependent on

Algorithm 2 Lithography friendly mandrel generation.

Require: A set of colored layer L

1: Select M_m and P_s from L: # either color is allowed.

2: # initial M_a in Sec. 4.2

3: **if** longer **then**

4: $M_{af} \leftarrow$ all direction expanding from P_s

5: **else if** shorter **then**

6: $M_{af} \leftarrow$ edge expanding from P_s

7: **else if** directional **then**

8: $M_{af} \leftarrow$ edge expanding from P_s

9: remove small island patterns from M_{af}

10: **end if**

11: # cut M_{af}

12: $Cm \leftarrow$ expanding M_m as much as $L_s + 2L_b$

13: $M_a \leftarrow M_{af} - C_m$

14: # postprocessing of M_a in Sec. 4.3

15: **for** each small feature $f \in M_a$ **do**

16: M_a merging or removal for manufacturability

17: define mandatory trim areas

18: **end for**

19: Metal retargeting in Sec. 5.2

20: DRC check with mask biasing, L_b

the resolution of an isolated pattern on a trim mask. Figure 15 shows a way for line-end control in the SADP process. By using our grouping and merging algorithm, the space between two line-ends can be merged so that the two lines become a united line in Fig. 15(b). Based on the modified layout, mandrel layout can be decided by layout coloring, and assist mandrel patterns are generated if needed in Fig. 15(c). Then the sidewall spacer patterns are generated near the mandrel patterns in Fig. 15(d). Finally, the target patterns on the wafer can be printed by eliminating unnecessary patterns using a trim mask since the space CD of the trim mask in Fig. 15(e) can be controlled by the trim mask OPC and other resolution enhancement technique approaches.

5.1.2 *T- or X-shapes*

As with LELE DPL, an island type of a T- or X-shaped pattern can be easily generated in the SADP process because there is not any coloring conflict when we choose the main mandrel layout. However, a T- or X-opened area might induce a coloring conflict as shown in Fig. 16. To resolve the layout conflict on mandrel patterns, we use grouping and merging approaches in Fig. 16(b), where the smallest merged region among several candidates to be merged can be selected.[26] This is because merging two conflicted polygons into one polygon the trim mask should remove the merged region at the cost of the mask overlay. Therefore, a shorter trim mask for removing the merged region is preferable for a smaller overlay impact on the second patterning.

By merging two conflict polygons in Fig. 16(b), the mandrel layout can be decided by layout coloring. Then, the sidewall spacer patterns are generated near the mandrel patterns in Fig. 16(c). Finally, the target patterns on the wafer can be printed by eliminating unnecessary patterns and the merged regions using a trim mask in Fig. 16(d). Note that the space of the merged region should be equal to or larger than the minimum space resolution of the trim mask. Therefore, if the merged region is smaller than the trim minimum resolution, we should modify the target design intent by iterating the layout design.

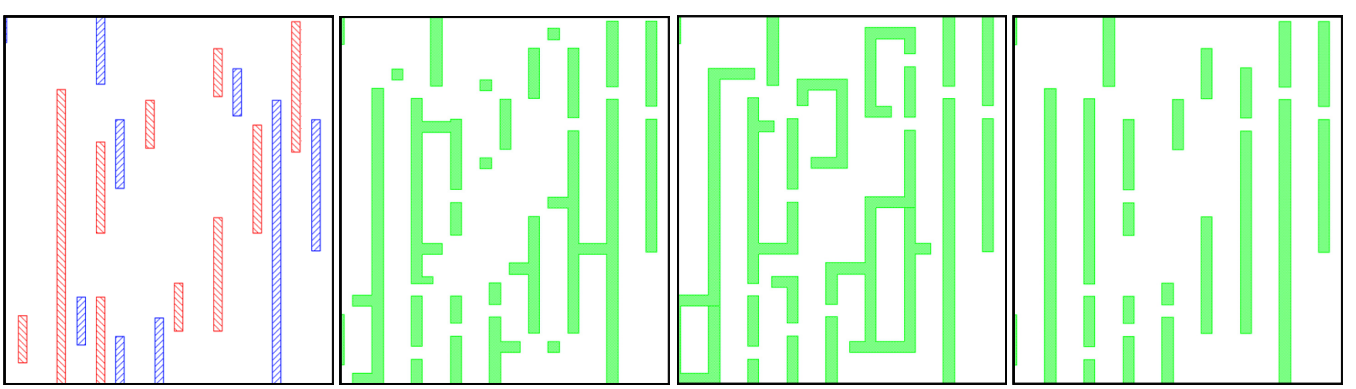

Fig. 13 Lithography friendly assist mandrel: where blue layout in (a) becomes main mandrel. (a) coloring, (b) shorter, (c) longer, (d) directional.

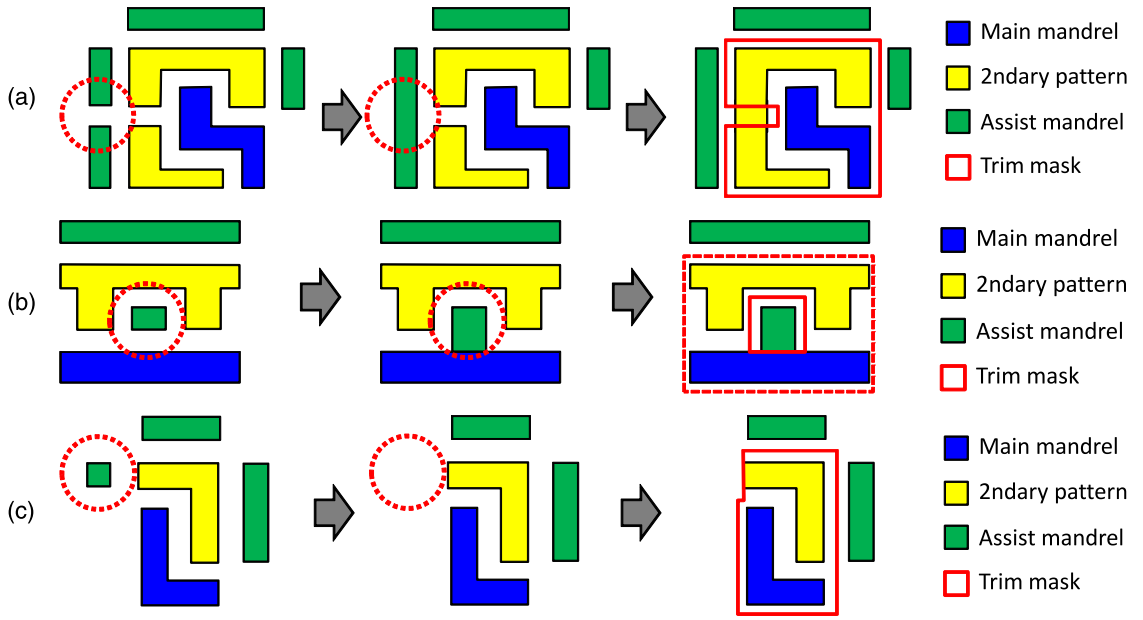

Fig. 14 Options of assist mandrel polygons: if the space among assist mandrels is smaller than a certain constraint, we can fill a space and combine the polygons. (a) mandrel filling, (b) merging with main mandrel or removing, (c) removing.

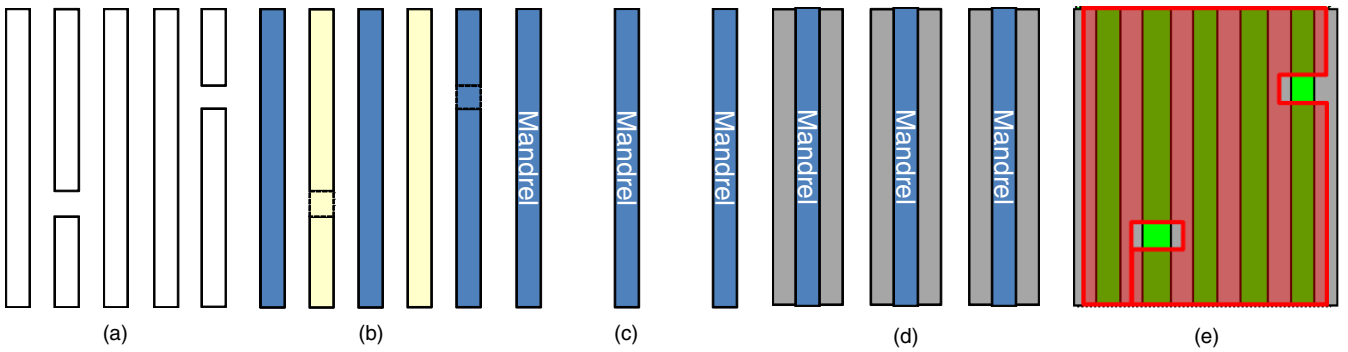

Fig. 15 Line-end: the space or width of the merged region should be equal or larger than the minimum space or width resolution of the trim mask. (a) target design, (b) color & grouping, (c) mandrel design, (d) sidewall spacer, (e) trim mask.

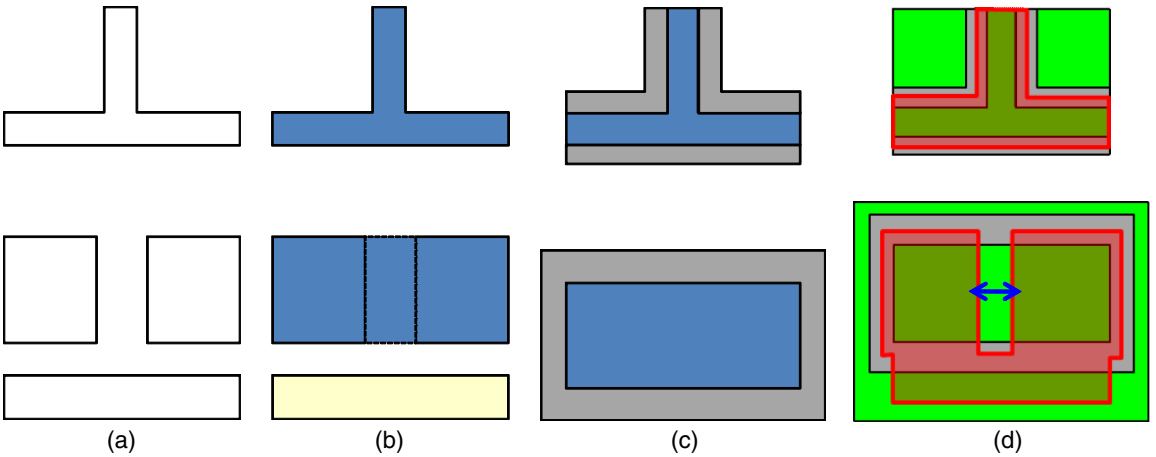

Fig. 16 T-shapes: the space or width of the merged region should be equal to or larger than the minimum space or width resolution of the trim mask. (a) target design, (b) color & grouping, (c) sidewall spacer, (d) trim mask.

5.1.3 *Narrow U-bend*

Short ranged U-bend shapes in LELE DPL can be patterned by introducing a "stitch" point.[1,8] However, in case there is more than one line just below the U-shape in Fig. 17, the layout cannot be decomposed due to a type of native conflict in LELE DPL.[24] Meanwhile, in SADP, short ranged U-shapes can be generated using the grouping and merging algorithm. By using our grouping and merging algorithm, the space between two patterns can be merged into one polygon in Fig. 17(b). Based on the mandrel layout, the sidewall spacer patterns are generated near the mandrel patterns in Fig. 17(c). Then the target patterns on the wafer can be printed by eliminating the merged regions using a trim mask in Fig. 17(d). The space of the merged region should be equal to or larger than the minimum space resolution of the trim mask. Therefore, if the merged region is smaller than the trim minimum resolution, we should modify the target design intent.

5.1.4 *Wide U-bend*

Long ranged U-bend shapes can be easily printed since the space of the U-shape is larger than the resolution of the first mandrel mask. In case there are some patterns in the space of the U-shape in Fig. 18, we can achieve wafer patterning using the grouping and merging approach. In the same fashion, the space of the merged region should be equal to or larger than the minimum space resolution of the trim mask.

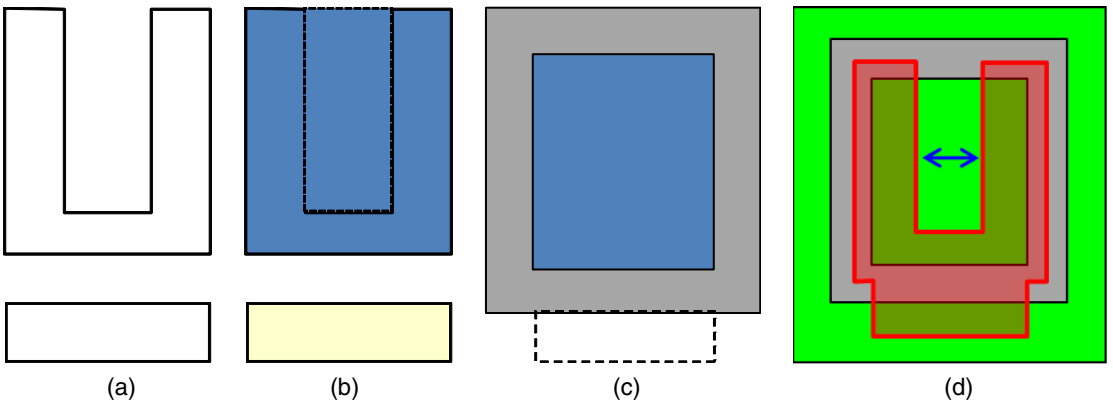

Fig. 17 U-bend (short range): the space or width of the merged region should be equal or larger than the minimum space or width resolution of the trim mask. (a) target design, (b) color & grouping, (c) sidewall spacer, (d) trim mask.

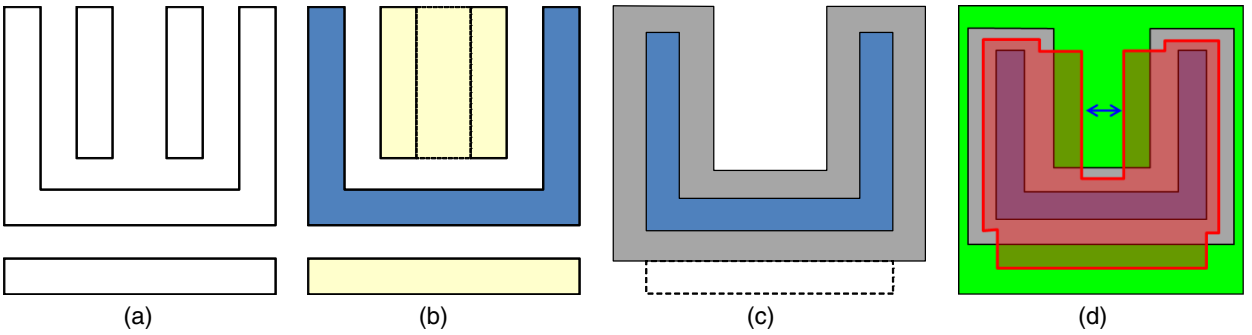

Fig. 18 U-bend (long range): the space or width of the merged region should be equal to or larger than the minimum space or width resolution of the trim mask. (a) target design, (b) color & grouping, (c) sidewall spacer, (d) trim mask.

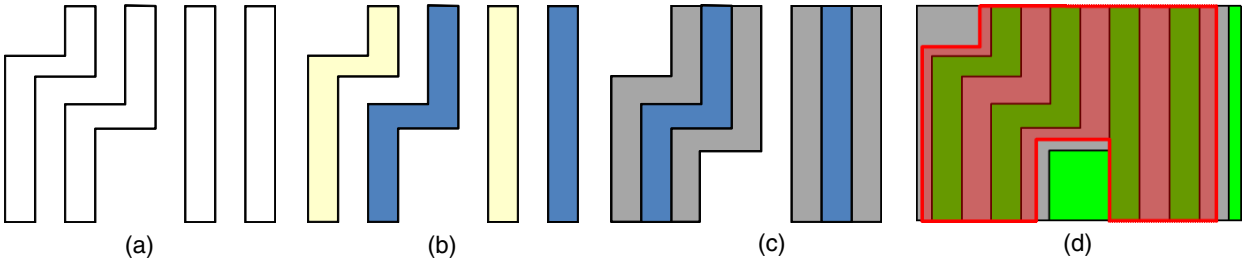

Fig. 19 Jogged features: the space or width of the merged region should be equal or larger than the minimum space or width resolution of the trim mask. (a) target design, (b) color & grouping, (c) sidewall spacer, (d) trim mask.

5.1.5 *Jogged features*

Even with the lithographic printability issue, jogged features are a usual pattern shape for layout routing. If layout patterns do not have any conflicts in layout coloring, SADP decomposition can be easily achieved. As shown in Fig. 19, the target design is subject to decomposing with two colors without any conflict in Fig. 19(b), which provides a robust core mask and trim mask layout in Figs. 19(c) and 19(d). The jogged layout shape may introduce assist mandrel patterns in order to support the secondary pattern.

5.1.6 *h-type jogged features*

h-type features are one of noncompliant layout types because they cause a noncolorable and nontrim friendly layout. In Fig. 20(a), an odd-cycle coloring conflict among the small island layout, jogged features, and their next straighten line is induced. Even with our grouping and merging algorithm, the second trim mask may introduce an MRC conflict due to smaller width and space. Just as for the feature types mentioned above, the space of the merged region in the core mask should be equal to or larger than the minimum space resolution of the trim mask.

5.2 *Layout Retargeting for SADP Compliant*

Since the width of a sidewall spacer is usually constant, in order to apply the SADP process to 2-D random logic, design retargeting is necessary. A design retargeting means to slightly modify the design intent in the layout, and it usually induces a slight increase of a metal width in the SID-type SADP. Slightly increased (thicker) metal lines give more benefits due to the following reasons: (1) The thicker metal line is better for timing issues, particularly for delays. Despite a small increase in coupling capacitance, a resistance decrease is more favorable for metal delay. (2) It is even better for lithography patterning. Thicker metal lines have more tolerance due to the lithography process.

As shown in Fig. 21(a), the space between the metal target and the mandrel is larger than the width of the spacer, and even worse, the space between the metal target and the spacer is somewhat narrower than the condition of the trim mask. If the metal layout allows retargeting of the design intent in Fig. 21(a), the width of the secondary pattern could be adjusted according to the space of the trim mask. As shown in Fig. 21, let S_{trm} be the space of the trim mask, S_{min} be the minimum allowable space of the trim mask, W_{mgn} be the trim mask overlay margin between the design intent and the sidewall spacer, W_{spr} be the sidewall spacer width, and W_{rtg} be the width of the allowable retargeting.

We assume in this paper that the space between the metal target and the mandrel is larger than the width of the spacer for defining the retarget condition. When $S_{\text{min}} \leq S_{\text{trm}}$, then no metal retarget is required because the trim mask can make a pattern of the metal target. Otherwise, a layout retarget for the metal target is necessary. Since W_{spr} and W_{mgn} are fixed in the SADP lithography process, the maximum retargeting width of the design intent, W_{rtg}, is defined as follows:

$$W_{\text{rtg}} = S_{\text{trm}} - (W_{\text{spr}} - W_{\text{mgn}}). \quad (1)$$

By introducing the maximal allowable retargeting width at the trim mask, we can have more flexibility in layout decomposition and lithography manufacturing in SADP.

6 Experimental Results

We implemented a mask decomposition automation for the SID-type SADP process and tested it with metal layers of industrial 22-nm node standard cells and 22-nm node logic devices. First, the minimum width, space, and sidewall spacer of 22-nm node standard cells are all 34 nm. The etch bias per edge for mandrels is 8 nm, which means the minimum width of the core mask for the first lithography

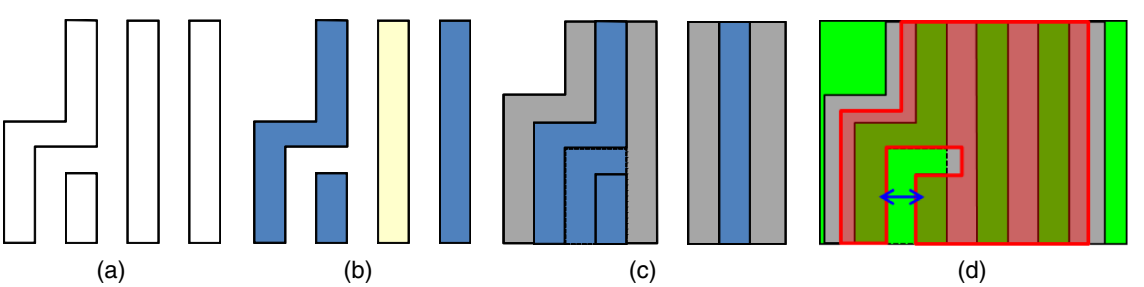

Fig. 20 Jogged features (h-type): the space or width of the merged region should be equal to or larger than the minimum space or width resolution of the trim mask. (a) target design, (b) color & grouping, (c) sidewall spacer, (d) trim mask.

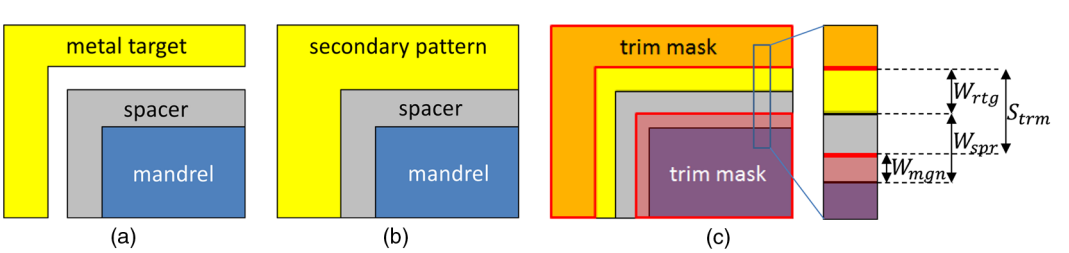

Fig. 21 Metal retargeting rule: (a) the space between the metal target and the mandrel is larger than the width of the spacer, (b) the secondary pattern is enlarged, (c) if S_{trm}, metal retargeting is applied.

patterning is 50 nm (34 nm + 2 × 8 nm). The minimum space of the core mask layout and the minimum width and space of the trim mask layout are all 50 nm. The overlay margin between the trim mask and the design intent is 5 nm in our experiments.

Figure 22 shows the results of our SADP decomposition for 22-nm node standard cells, which are already finished with proper placement and routing designs. As shown in Fig. 22(a), the layout has multiple widths and spaces, and the shape of the layout looks arbitrary so that the mask decomposition for the SADP process is challenging. Based on our layout coloring for SADP decomposition, we select the main mandrel by considering the trim mask layout and define the assist mandrel layout in Fig. 22(b). After making the core layout without any DRC violations, we shrink the core layout with the following etch step, and then generate the sidewall spacer pattern nearby the mandrel in Fig. 22(b). The trim mask patterning is followed by the BARC deposition in Fig. 22(c), then we can get the final patterning after some etch processing in Fig. 22(d). As Fig. 22(d) shows, the final metal pattern meets the target design with slightly thicker patterns due to the retargeting rule.

The SADP results of SRAM memory array, where specific polygons are repeating are shown in Fig. 23. Based on our layout coloring engine, the layout was assigned into different colors by keeping the core mask design constraints in Fig. 23(b). The coloring engine analyzes the design intent and finds all critical spaces to be in the *X* direction, meaning that decomposition has to focus on this

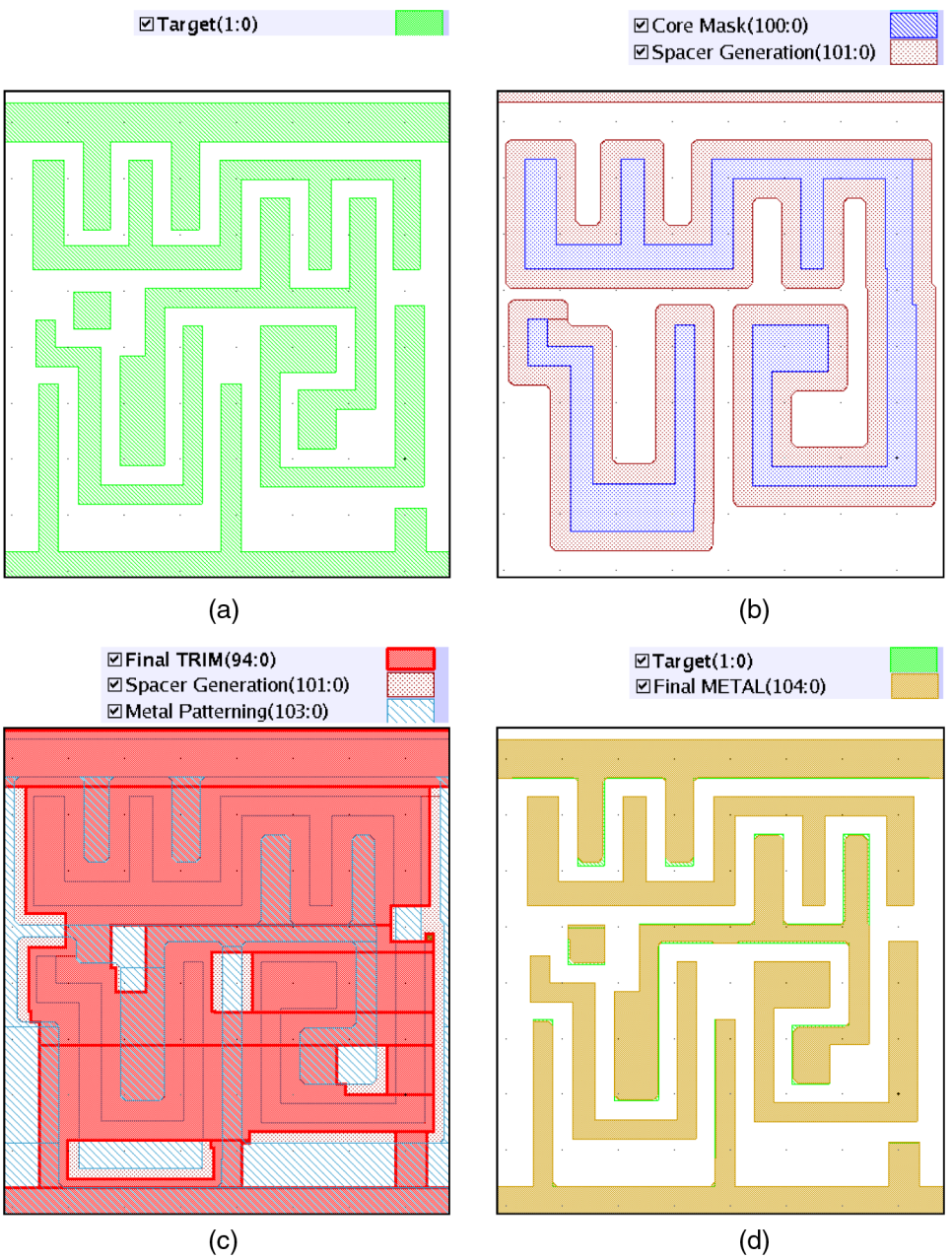

Fig. 22 SADP layout decomposition on 22-nm standard cells. (a) Target layer, (b) mandrel & spacer, (c) trim mask, (d) final patterns.

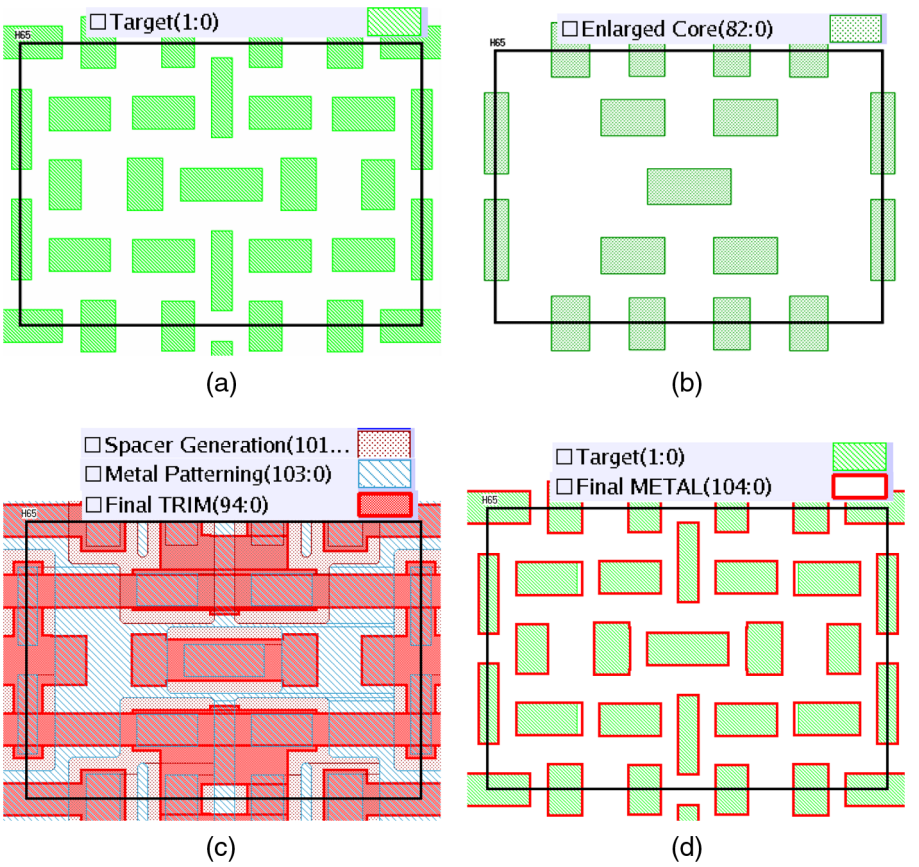

Fig. 23 SADP layout decomposition on SRAM cell. (a) Target layer, (b) mandrel & spacer, (c) trim mask, (d) final patterns.

direction. Since no coloring conflicts were found in the memory array, the trim mask could be generated without any mask rule violations in Fig. 23(c) and the final patterns were successively matched with the design intent in Fig. 23(d). The estimated final patterning was slightly different from the design intent because we applied metal retargeting for SADP flexibility since the width of the sidewall spacer is usually constant.

We also tested our SADP layout decomposition for an industrial 22-nm node full-chip logic metal layer. Eight layout blocks which have the same area (20 μm × 20 μm) are evaluated. The minimum width and space of the layout are

Table 1 DRC error on both the core mask and the trim mask with the proposed different layout coloring approaches.

	EDGE[a]		STST[a]			TMFC[a]		
Layout	Core	Trim	Core	Trim	Improve%[b]	Core	Trim	Improve%[b]
Layout1	2	13	2	10	23.08	2	3	76.92
Layout2	1	25	1	19	24.00	0	5	80.00
Layout3	2	32	2	29	9.38	0	12	62.50
Layout4	0	34	0	29	14.71	0	10	70.59
Layout5	0	18	0	16	11.11	0	9	50.00
Layout6	2	31	2	27	12.90	1	14	54.84
Layout7	3	31	3	28	9.68	2	11	64.52
Layout8	1	34	1	32	5.88	1	12	64.71
Average	1.4	27.3	1.4	23.8	13.84	0.8	9.5	65.51

[a]EDGE: edge segment-based coloring. STST: EDGE + shortest-path coloring. TMFC: STST + self-conflict coloring + trim friendly coloring.
[b]Improvement the errors on the trim mask from EDGE.

35 and 45 nm, respectively. The width of a sidewall spacer is 45 nm, and the etch bias per edge for mandrels and the overlay margin of the trim mask are all 5 nm. The minimum width and space of the trim mask are 45 and 55 nm, respectively. We used a commercial tool for model-based OPC and lithography simulation. Our optical parameters are wavelength = 193 nm, numerical aperture (NA) = 1.25 immersion, and dipole illumination $\sigma = 0.85/0.55$. Following industrial practices, we first performed full OPC for all mask layouts and ran a lithography simulation with a process variation: focus = ± 50 nm.

Table 1 shows the number of DRC errors on both the core mask and trim mask with the proposed different layout coloring approaches: the edge segment–based coloring (EDGE) in Fig. 5, the shortest-path coloring (STST) in Sec. 3.3, and the mask friendly coloring (TMFC) in Sec. 3.5. The DRC conflicts mean both width and space violations given the minimum requirement for the core and the trim masks. The DRC conflicts of the core mask are very small, yet the TMFC has slightly fewer conflicts than other approaches. Meanwhile, the improvements on the trim mask are large when we use TMFC. STST at the trim mask has around a 14% improvement, yet TMFC has as much as a 65% improvement on average compared with EDGE. Table 1 shows that our SADP automation can decompose random 2-D layout with just a few DRC conflicts, which can be easily fixed by slightly modifying the target design.

Next, we compared various approaches of the mandrel generation and evaluated lithographic printability in Table 2: a shorter, longer, and directional mandrel in

Table 2 Lithographic printability check with the proposed different approaches of the mandrel generation.

	Shorter mandrel			Longer mandrel			Directional mandrel		
	BF[a]	DF[a]		BF[a]	DF[a]		BF[a]	DF[a]	
Layout	3-nm EPE[b]	6-nm EPE[b]	Fail[b]	3-nm EPE[b]	6-nm EPE[b]	Fail[b]	3-nm EPE[b]	6-nm EPE[b]	Fail[b]
Layout1	139	44	20	459	397	0	27	55	0
Layout2	216	54	3	669	593	1	15	52	0
Layout3	137	45	4	547	477	0	9	44	0
Layout4	111	68	0	502	473	0	9	70	0
Layout5	135	61	1	503	411	1	14	58	0
Layout6	138	71	2	536	438	2	15	66	0
Layout7	141	52	9	558	466	2	25	51	0
Layout8	91	39	1	451	401	0	5	40	0
Average	139	54.3	5	528	457	0.8	14.9	54.5	0

[a]BF: at the best focus, DF: at the out focus variation.
[b]3 nm: 3 nm < EPE, 6 nm: 6 nm < EPE, F: # of patterning fail.

Table 3 Comparison of the lithographic printability with litho-etch-litho-etch (LELE) double-patterning technology (DPT).

	LELE DPT				Self-aligned double patterning			
	BF[a]	DF[a]		Stitch	BF[a]	DF[a]		Stitch
Layout	3-nm EPE[b]	6-nm EPE[b]	9-nm EPE[b]		3-nm EPE[b]	6-nm EPE[b]	9-nm EPE[b]	
Layout1	537	715	515	109	28	40	35	0
Layout2	822	1101	746	143	16	39	13	0
Layout3	626	833	598	148	9	39	12	0
Layout4	635	855	644	167	9	64	25	0
Layout5	541	750	525	78	14	43	24	0
Layout6	703	937	705	115	16	55	26	0
Layout7	666	948	671	87	26	40	20	0
Layout8	610	916	551	151	7	38	2	0
Average	642.5	881.9	619.4	125	15.6	44.8	19.6	0

[a]BF: at the best focus, DF: at the out focus variation.
[b]3 nm: 3 nm < EPE, 6 nm: 6 nm < EPE $\leq$ 9 nm, 9 nm: 9 nm < EPE, S: # of stitch.

Fig. 13 in Sec. 4.2. After performing OPC and lithography simulation, we calculated edge placement error (EPE) of the printed image. EPE is a popular metric with which to evaluate lithography simulated images. It means the difference between the resulting simulated image and the target design of an edge of the layout. We measured the number of locations with an EPE larger than 3 nm at the best process conditions, and 6 nm at the out-focus (defocus) process conditions. The longer mandrel shows the largest EPE at the both the best and defocus conditions. This is because the longer mandrel has more horizontal and vertical patterns and some patterns are not well printed by dipole illumination. However, when we use the longer mandrel for the core mask, the patterning failures, in particular, missing small island patterns, are decreased compared to the shorter mandrel. It implies that the shorter mandrel is prone to removal at the first patterning. Meanwhile, when we applied the directional mandrel to the core mask, we achieved a much smaller EPE variation without failing patterns. Even though the EPE may be dependent on input lithographic conditions, in our experiments, the directional mandrel is the best option for the core mask in SID SADP decomposition.

Last, we compared the lithographic printability of SADP with that of LELE in Table 3. The mask decomposition of LELE was performed by Proteus-DPT from Synopsys. According to Ref. 18, since the second mask of LELE suffers from wafer topography effects, the lithographic process tolerance of LELE is around 30% less than that of SADP. Thus, we put more focus variation into the second mask of LELE, then counted the number of EPE variations of both masks. The result shows that SADP has a much smaller patterning variation despite not having stitch points. Thus, we can say that SADP is promising for metal and other random layout patterning at the next lithography node.

7 Conclusion

In conclusion, we have shown several methods and options to produce manufacturable mask decompositions for sub-10-nm random metal layers with the SID style of SADP. The value of intelligent optimization methods for core and trim masks in SID SADP is clearly seen. Experimental results with industry designs show that the layout decomposition of SADP for a 2-D random layout is promising for the future of lithography patterning.

Acknowledgments

The authors are grateful for helpful discussions with Kevin Lucas, Gerry Luck-Pat, Ben Painter, and Levi Barnes of Synopsys, USA. We also thank Chul-Hong Park, Myung-Soo Noh, and Beom-Seok Seo of Samsung, Korea, for their support.

References

1. J. Yang et al., "A new graph theoretic, multi objective layout decomposition framework for double patterning lithography," in *Proc. Asia South Pac. Design Automation Conf.*, Taipei, Taiwan (2010).
2. Y. Ban et al., "Electrical impact of line-edge roughness on sub-45 nm node standard cells," *J. Micro/Nanolith. MEMS MOEMS* **9**(4), 041206 (2010).
3. Y. Ban, S. Sundareswaran, and D. Pan, "Modeling and characterization of contact-edge roughness for minimizing design and manufacturing variations," *J. Micro/Nanolith. MEMS MOEMS* **9**(4), 041211 (2010).
4. M. Gupta, K. Jeong, and A. Kahng, "Timing yield-aware color reassignment and detailed placement perturbation for bimodal CD distribution in double patterning lithography," *IEEE Trans. on Comput.-Aided Des. Integr. Circuits Syst.* **29**, 1229–1242 (2010).
5. J. Finders et al., "Double patterning lithography for 32 nm: critical dimensions uniformity and overlay control considerations," *J. Micro/Nanolith. MEMS MOEMS* **8**, 011002 (2009).
6. D. Carau et al., "Advanced metrology for the 14 nm node double patterning lithography," *Proc. SPIE* **9132**, 91320D (2014).
7. Y. Chang et al., "Full area pattern decomposition of self-aligned double patterning for 30-nm node NAND FLASH process," *Proc. SPIE* **7637**, 76371N (2010).
8. M. Cho, Y. Ban, and D. Pan, "Double patterning technology friendly detailed routing," in *Proc. Int. Conf. on Computer Aided Design*, San Jose, California (2008).
9. A. Kahng et al., "Layout decomposition for double patterning lithography," in *Proc. Int. Conf. on Computer Aided Design*, San Jose, California (2008).
10. G. Bailey et al., "Double pattern EDA solutions for 32 nm HP and beyond," *Proc. SPIE* **6521**, 65211K (2007).
11. W. Arnold, "Double-patterning lithography," *J. Micro/Nanolith. MEMS MOEMS* **8**, 011001 (2009).
12. J. Yang and D. Pan, "Overlay aware interconnect and timing variation modeling for double patterning technology," in *Proc. Int. Conf. on Computer Aided Design*, San Jose, California (2008).
13. C. Ausschnitt and S. Halle, "Combinatorial overlay control for double patterning," *J. Micro/Nanolith. MEMS MOEMS* **8**, 011008 (2009).
14. L. Liebmann et al., "Taming the final frontier of optical lithography: design for sub-resolution patterning," *Proc. SPIE* **7641**, 764105 (2010).
15. I. Kamohara and T. Schmoeller, "Split, overlap, stitching, and process design for double patterning considering local reflectivity variation by using rigorous three-dimensional wafer-topography and lithography simulation," *J. Micro/Nanolith. MEMS MOEMS* **10**, 023013 (2011).
16. I. Kamohara and T. Schmoeller, "Split, overlap/stitching, and process design for double patterning considering local reflectivity variation by using rigorous 3D wafer-topography/lithography simulation," *Proc. SPIE* **7274**, 72740H (2009).
17. J. Siebert et al., "Analysis of topography effects on lithographic performance in double patterning applications," *Proc. SPIE* **7274**, 72740M (2009).
18. Y. Ma et al., "Decomposition strategies for self-aligned double patterning," *Proc. SPIE* **7641**, 76410T (2010).
19. M. Mirsaeedi, J. Torres, and M. Anis, "Self-aligned double patterning (sadp) layout decomposition," in *Proc. Int. Symp. on Quality Electronic Design*,San Jose, California (2011).
20. F. Chen et al., "Sidewall profile engineering for the reduction of cut exposures in self-aligned pitch division patterning," *J. Micro/Nanolith. MEMS MOEMS* **13**, 011008 (2014).
21. W. Shiu et al., "Advanced self-aligned double patterning development for sub-30-nm DRAM manufacturing," *Proc. SPIE* **7274**, 72740E (2009).
22. Y. Ban et al., "Layout decomposition of self-aligned double patterning for 2D random logic patterning," *Proc. SPIE* **7974**, 79740L (2011).
23. D. Pan, B. Yu, and J. Gao, "Design for manufacturing with emerging nanolithography," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **32**(10), 1453–1472 (2013).
24. K. Yuan, J. Yang, and D. Z. Pan, "Double patterning layout decomposition for simultaneous conflict and stitch minimization," in *Proc. Int. Symp. on Physical Design*, San Diego, California (2009).
25. K. Agarwal, "Frequency domain decomposition of layouts for double dipole lithography," in *Proc. Design Automation Conf.*, Anaheim, California (2010).
26. Y. Ban, K. Lucas, and D. Pan, "Flexible 2D layout decomposition framework for spacer-type double pattering lithography," in *Proc. Design Automation Conf.*, San Diego, California (2011).

Yongchan Ban received his PhD degree in electrical and computer engineering from the University of Texas at Austin in 2011. He is now a principal research engineer in LG Electronics, Republic of Korea. He was a senior software engineer with Intel Corporation and Samsung Electronics. He has published around 60 papers and is the holder of 5 patents. His research interests include nanometer VLSI physical design, design for manufacturing, and design/CAD for emerging technologies.

David Z. Pan received his BS degree from Peking University, and MS and PhD degrees from the University of California, Los Angeles, in 2000. Currently, he is engineering foundation professor at the Department of Electrical and Computer Engineering, University of Texas at Austin. He has published over 200 papers in refereed journals and conferences and is the holder of 8 U.S. patents. He has received a number of awards, including SRC Technical Excellence Award. He is an IEEE Fellow.