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Invited Paper

Toward Unidirectional Routing Closure in Advanced Technology Nodes

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Abstract: In advanced technology nodes, unidirectional layout is strongly preferred for high-density metal layers for better manufacturability. The lithography printing of unidirectional layout can be tightly controlled with illumination source optimization and resolution enhancement techniques. Meanwhile, with the unidirectional layout, self-aligned double and quadruple patterning can be applied to achieve finer pitches beyond the resolutions limits of 193 nm lithography tools. However, unidirectional layout style introduces significant impacts on the physical design flow. Notably, unidirectional routing limits the standard cell pin accessibility, which makes manual cell layout design and optimization more and more challenging under modern standard cell architecture. In the routing phase, routing densities and resource competitions on lower metal layers are becoming increasingly high, where intelligent approaches are needed to resolve routing resource competitions for unidirectional routing closure. Moreover, post-routing optimization is inevitable to avoid significant engineering-changing-efforts for unidirectional routing under advanced manufacturing constraints. In this paper, we present a holistic approach, including standard pin access evaluation/optimization, pin access and routing co-optimization and post-routing optimization, to enable unidirectional routing closure in advanced technology nodes.

Keywords: unidirectional layout, multiple patterning, pin access, routing interval, redundant local loop

1. Introduction

As the technology node scales down to 10 nm node and beyond, minimum feature size of the manufacturing process has been shrinking beyond the resolution limits of 193 nm lithography tools. Due to the delay of emerging lithography techniques, such as extreme ultraviolet lithography (EUVL), electron-beam lithography (E-beam) and directed self-assembly (DSA), multiple patterning lithography (MPL) has been widely adopted in semiconductor industry to further push the geometric scaling in advanced technology nodes. In general, there exist two types of MPL, Litho-Etch-Litho-Etch (LELE) type and self-aligned type. LELE-type of MPL allows stitch insertions and two-dimensional patterns [27], [59], [70], [71], [77], but coloring and overlay compensation schemes become extremely complicated for triple patterning lithography and beyond [12], [15], [30], [38], [60], [73], [76], [81]. Self-aligned type of MPL can minimize electrical variations from overlay and line-edge-roughness but introduces complex coloring and line-end constraints [40], [42], [56].

MPL generates a significant amount of design complexities, such as coloring, overlay and line-end rules, into the physical design flow. The industrial routine for standard cell design still follows handcrafted design and optimization, which allows occasional two-dimensional layout patterns on metal-1 (M1) layer and below through extensive engineering changing efforts [33], [54]. This makes the standard cell design and placement stages particularly important to resolve manufacturing constraints, especially coloring, on M1 layer and below [14], [17], [19], [74]. In the routing phase, for upper metal layers with relaxed pitches and low metal densities, each layer has a preferred routing direction and two-dimensional routing patterns, i.e., wire bending, can be used to provide flexible routing solutions. However, for lower metal layers with tight pitches and high metal densities, unidirectional layout forbids wire bending on a single metal layer and switching routing directions means changing routing layers. For detailed routing closure on high-density metal layers, unidirectional layout style with simplified design-for-manufacturing schemes remains as the mainstream routine in advanced technology nodes [21], [51], [52], [54], [75]. The single-mask lithography printing of unidirectional layout can be tightly controlled using illumination source optimization and resolution enhancement techniques [56]. This also simplifies MPL-related coloring constraints. Specifically, track-based coloring scheme assigns each layout pattern an implicit color before layout patterns are created. This significantly reduces the coloring complexities for a physical design tool because each layout pattern created by the tool automatically has a legal coloring solution. However, unidirectional layout style still induces a set of challenging restrictions, such as sophisticated metal line-end rules and lower metal layer routing with high-density layout patterns. This further induces routing-limited scaling in predictive 7 nm technology node, which means routing densities and routing resource competitions on lower metal layers are becoming increasingly high, such that design area has to be relaxed to obtain routing closure [33].

In advanced technology nodes, a standard cell architecture de-

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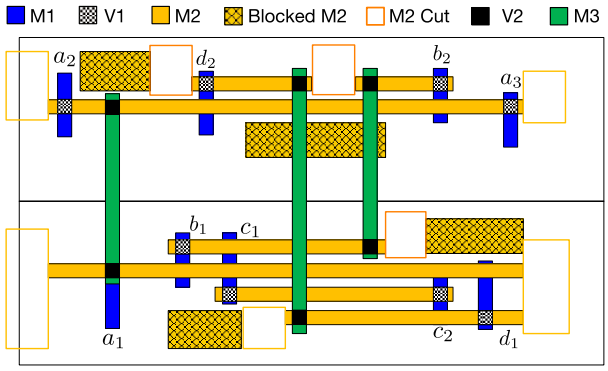

Fig. 1 Unidirectional routing on high-density metal layers.

cides that only a finite number of routing tracks are available to access each standard cell I/O pin. Therefore, it is very important to allocate the routing tracks on top of standard cell I/O pins in an intelligent and efficient manner so that all I/O pins can be accessed for routing closure. An example of unidirectional routing on M2 and metal-3 (M3) layers is shown in **Fig. 1** [*1]. This routing instance includes 4 net connections, i.e., (a_1, a_2, a_3), (b_1, b_2), (c_1, c_2) and (d_1, d_2). The routing patterns for net connections are purely unidirectional and need to be packed within a finite number of horizontal routing tracks, which leads to high routing density on M2 layer.

A router is required to follow complex line-end rules and generate lithography-friendly cut patterns (only M2 cuts are shown here for clearance). During the manufacturing procedure, unidirectional lines are first patterned with self-aligned type of MPL, where unwanted portions of the layout will be removed using cut patterns, such as M2 cuts in Fig. 1. The cut patterns can be manufactured using 193 nm lithography [56], MPL [16] or other emerging lithography options, such as E-beam [10] and DSA [61] to improve metal pattern density and the printability of metal line ends. In general, unidirectional layout and high routing density result in severe routing resource competitions. Meanwhile, advanced manufacturing constraints for lithography-friendly cut mask designs translate to complex metal line-end rules, which further introduce complicated neighborhood interactions among routing patterns. These restrictions aforementioned make unidirectional routing closure only possible with significant engineering-changing-efforts. Therefore, it is important for physical design tools to deliver automatic routing closure or at least high-quality routing results within affordable runtime.

We present a holistic physical design flow to effectively enable unidirectional routing closure. Our approach includes standard cell design with pin access evaluation and optimization, pin access and routing co-optimization and post-routing optimization. In the standard cell level, designers handcraft cell layout to optimize I/O pin shapes for better pin accessibility, i.e., increase the number of hit points available for a router. However, manual optimization has limited capabilities without the assistance from physical design tools because of complex pin-to-pin interference under advanced manufacturing constraints. Thus, a standard cell pin accessibility evaluation engine is presented to provide quick feedbacks to designers for better I/O pin optimizations. In the routing phase, pin access interference is effectively and efficiently resolved by pin access planning schemes and routing interval generation and assignment techniques. A negotiation-congestion-based router is adopted for better routing closure. To avoid significant engineering-changing-efforts, post-routing optimization techniques are discussed to enhance the manufacturing yield and generate manufacturing-friendly cut/trim mask designs for unidirectional routing closure.

The rest of this paper is organized as follows. Section 2 introduces relative background on unidirectional routing layout and advanced manufacturing constraints, along with the holistic flow to enable unidirectional routing closure. Section 3 presents standard cell architecture and design approaches to address the impact of unidirectional layout on standard cell pin accessibility. Section 4 presents advanced routing schemes with unidirectional layout, with emphasis on handling pin access interference. Section 5 discusses the post-routing optimization techniques to avoid significant engineering-changing-efforts for unidirectional routing closure. Section 6 briefly summarizes the holistic approach for unidirectional routing closure and discusses promising research directions to further enhance the design closure in advanced technology nodes.

2. Unidirectional Routing Basics and Flow

In advanced technology nodes, routing patterns on lower metal layers are purely unidirectional due to restrictive design-for-manufacturing constraints. Meanwhile, density scaling implies that same number of net connections need to be compacted within smaller area compared to that of previous technology nodes. To obtain unidirectional routing closure, we need a holistic approach to handling routing resource competitions while accommodating advanced manufacturing constraints. We first discuss unidirectional layout in Section 2.1 and advanced manufacturing constraints in Section 2.2. We further propose a unidirectional routing closure flow in Section 2.3.

2.1 Unidirectional Layout

In advanced technology nodes, layout regularity and multiple patterning lithography are the key to the geometric scaling on lower metal layers [34], [40], [56]. Unidirectional layout style simplifies the layout coloring scheme and is manufacturing-friendly to the self-aligned type of MPL [40], [42]. An example is shown in **Fig. 2**, where target patterns are purely unidirectional in Fig. 2 (a). Figure 2 (b) illustrates a track-based coloring scheme for SADP, where neighboring routing tracks are assigned different colors, i.e., light blue for mandrel layout and yellow for sub-metal. Suppose the M2 pitch is 48 nm for 10 nm technology node, the minimum pitch of mandrel layout in Fig. 2 (b) is 96 nm, which is within the resolution limits of 193 nm lithography tools [63]. During the manufacturing process, the mandrel layout is first patterned with 193 nm lithography tools. Then, spacer materials are deposited around mandrel layout, where the gaps between neighboring spacers define sub-metal patterns. The layout patterns defined by mandrel and sub-metal in Fig. 2 (c) or Fig. 2 (d) include undesired portions compared to the target patterns in Fig. 2 (a).

[*1] In advanced technology nodes, metal-1 layer is typically not available for detailed routing due to complex spacing and coloring constraints.

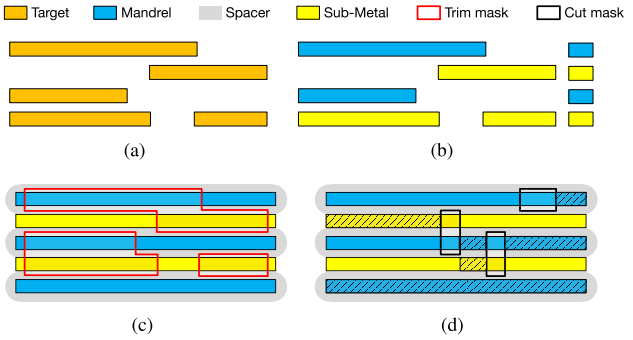

Fig. 2 (a) Target patterns, (b) track-based coloring, (c) SADP with trim masks, (d) SADP with cut masks [62].

Thus, trim or cut masks are inserted to remove undesired portions and obtain manufactured patterns close to target patterns as shown in Fig. 2 (c) and (d). Specifically, the SADP with trim and cut mask schemes define target patterns with the geometric Boolean functions – Trim mask *NOT* Spacer and (Mandrel *OR* Sub-metal) *NOT* Cut Mask, respectively.

Trim or cut masks can be patterned with 193 nm lithography or other emerging lithography techniques, such as EUVL, E-beam and DSA. Physical design tools or layout designers need to follow lithography-dependent design rules, such as minimum width or spacing rule, to make trim or cut masks compliant with their lithography options. Therefore, line-end extension techniques have been widely used to improve layout printability [78], [79]. For instance, dummy patterns (dashed light blue and dashed yellow patterns) are added in Fig. 2 (d) to obtain a 193 nm lithography-friendly cut mask design. The manufacturing procedure aforementioned can be easily extended to more complex patterning schemes, such as SAQP, once related design rules are defined [11].

2.2 Advanced Manufacturing Constraints

Routing closure on lower metal/via layers is particularly challenging due to their complex manufacturing constraints. For lower metal layers, the minimum width or spacing rules for trim/cut masks introduce metal line-end rules across multiple routing tracks. An example of metal line-end rules is shown in **Fig. 3** (a), where design rules are applied to metal patterns on neighboring routing tracks with SADP [39], [42]. For lower via layers, self-aligned via [3], [53] and via density constraints [25] are particularly important for manufacturing high-density via patterns in advanced technology nodes. The pitch of neighboring vias in Fig. 3 (b) is beyond the resolution limit of 193 nm lithography. Self-aligned via manufacturing technique first forms groups of vias and further separates them by self-aligned manufacturing tricks, which represents another paradigm of via density scaling [3], [53].

The design constraints aforementioned are elementary pieces of manufacturing complexities in advanced technology nodes [18]. Practical manufacturing solutions could be much more complex and foundry dependent [24], [44]. However, unidirectional layout style with complex metal line-end and via design constraints remains a promising candidate for geometric scaling in advanced technology nodes, which also makes the

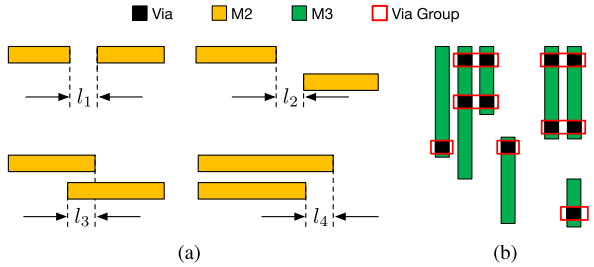

Fig. 3 (a) Metal line-end design rules [40], [64], (b) self-aligned via groups [3], [53].

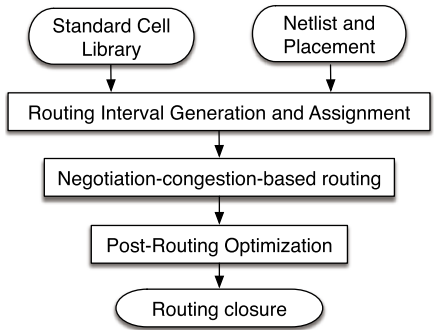

Fig. 4 Unidirectional routing flow.

unidirectional routing closure on lower metal layers extremely challenging.

2.3 Routing Closure Flow

To obtain unidirectional routing closure, we present a holistic approach in **Fig. 4**, which includes standard cell design, routing and post-routing optimization. At the standard cell level, pin accessibility is a major bottleneck for unidirectional closure under advanced manufacturing constraints. To improve standard cell pin access, one option is to go through the design flow in Fig. 4, which detects hard-to-route cells for iterative standard cell library optimization [33]. However, this approach results in large turnaround time and could be design dependent, which motivates searches for other alternatives. Therefore, a standard cell pin access optimization/evaluation engine is proposed, which guides standard cell designers to provide maximized pin accessibility for the router. In the routing level, routing interval generation and assignment are presented to resolve routing resource competitions on lower metal layers. Then, a negotiation-congestion based routing scheme is adopted to achieve manufacturing-friendly routing patterns. In post-routing stage, we discuss a redundant local-loop insertion technique for the yield enhancement of unidirectional routing patterns. Cut/trim mask redistributions are further enabled by line-end extension techniques while accommodating complex metal line-end rules for different lithography options.

3. Standard Cell Pin Access Optimization

Standard cell library design is the foundation of the entire physical design flow, which makes it critical to the high-quality design closure, especially to the unidirectional routing closure on lower metal layers. Due to continued geometric scaling in 10 nm node and beyond, physical design tools need to access standard cell I/O pins in congested areas under restrictive design rules as

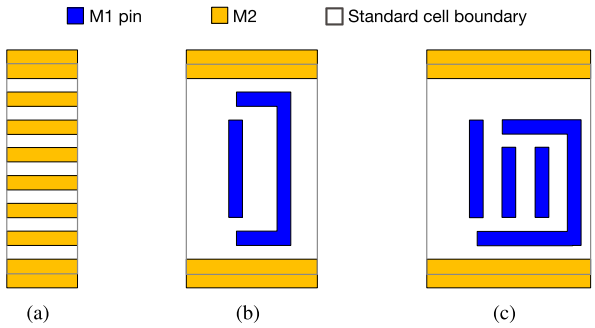

Fig. 5 Standard cell architecture, (a) 7.5 M2 track architecture, (b) "Inverter" layout on M1 and M2, (c) "AND-OR-Inverter" layout on M1 and M2 [33].

discussed in Section 2.2. Although standard cell designers try to optimize I/O pin shapes under unidirectional routing style, human-driven optimization is becoming increasingly difficult due to complex pin-to-pin interference under advanced manufacturing constraints. In this section, we present a standard cell pin access optimization/evaluation engine under state-of-the-art standard cell architecture.

3.1 Standard Cell Architecture

Due to complex design-for-manufacturing constraints, there are finite options of standard cell architecture for a specific advanced technology node [6], [33], [55]. **Figure 5** illustrates a 7.5-track standard cell architecture at 7 nm technology node. A standard cell architecture pre-determines cell height in the number of M2 routing tracks. The standard cell boundary decides the region of intra-cell layout patterns on M1 and lower manufacturing layers, which are used for intra-cell connections and standard cell I/O pins. While occasional M2 usages are allowed for intra-cell connections for complex standard cells [63], M2 and upper layers are mainly used for routing connections. Regular M2 tracks in the middle of Fig. 5 (a) are routing tracks fed into a router for net connections. Thick M2 tracks on the top and bottom of standard cell boundary align with the power/ground rails of a specific design. The M1 I/O pins of "Inverter" and "AND-OR-Inverter" are shown in Fig. 5 (b) and (c), respectively. In the routing level, these M1 I/O pins can only be accessed with fixed number of M2 routing tracks. As M2 routing patterns are purely unidirectional, there exists a limited number of M2 accessing points (see **Fig. 6** (b)) for each I/O pin, which makes routing density and resource competition increasingly high on lower metal layers. This makes standard cell pin access optimization on lower metal layers particularly important for unidirectional routing closure.

3.2 From Hit Points to Hit Point Combinations

We first present the following definitions for standard pin access issue [63], [64].

Definition 1 (Hit Point) *The overlap of an M2 routing track (pre-determined by standard cell architecture) and an I/O pin shape is defined as a Hit Point for that particular I/O pin.*

Definition 2 (Hit Point Combination) *A set of hit points (with a defined access direction–left or right) where each I/O pin in a standard cell is accessed exactly once is defined as a Hit Point Combination for that cell.*

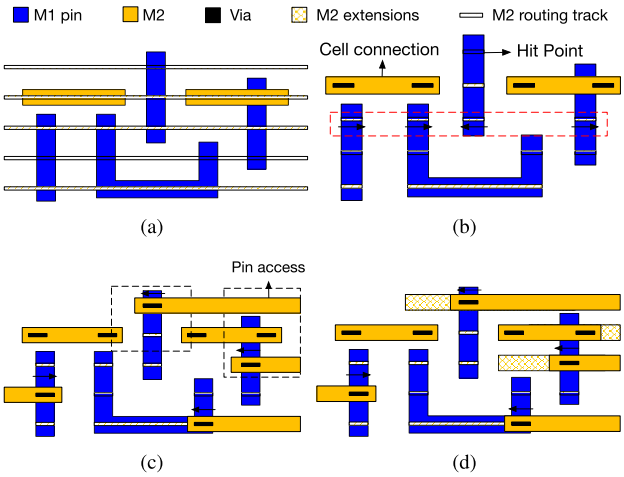

Fig. 6 (a) M1 I/O pins and M2 routing tracks, (b) hit points and M2 usage for within-cell connections, (c) a hit point combination with M2 pin access patterns, (d) M2 pin access patterns with line-end extensions [64].

An example of complex standard cell design is shown in Fig. 6 (a), where M2 routing tracks are running horizontally. For each I/O pin, hit points, given by Definition 1 can be extracted from the overlaps of M2 routing tracks and M1 I/O pins in Fig. 6 (b). The set of hit points in Fig. 6 (c) is a hit point combination, given by Definition 2, where each hit point is associated with one I/O pin. The mainstream industrial routine for standard cell design has been handcrafted design and optimization. For better pin accessibility, a standard cell designer mainly focuses on increasing the vertical span of an M1 pin (assuming horizontal M2 routing tracks), which provides more hit points for each pin during routing stage [33]. In advanced technology nodes, this technique is becoming less effective due to a finite number of M2 routing tracks and pin-to-pin interference [6], [64]. To systematically evaluate pin accessibility under pin-to-pin interference and advanced manufacturing constraints, it is important to quantify pin accessibility in terms of "hit point combinations" and "hit points" simultaneously [64]. The number of hit points quantifies the pin accessibility of a single I/O pin in isolation, while the number of hit point combinations evaluates the pin accessibility of entire cell with pin-to-pin interference under advanced manufacturing constraints. Thus, hit point combination provides a more direct metric for designers to optimize I/O pin shapes for better standard cell pin accessibility. The key idea is that pin-to-pin interference needs to be explicitly considered during pin accessibility evaluation. The similar idea applies to both intra-cell and inter-cell pin accessibility evaluation at the placement stage [58], [68].

3.3 Pin Access Evaluation and Optimization

We present a standard cell pin access optimization and evaluation engine, which provides quick feedbacks of pin accessibility to standard cell designers. A hit point combination is determined to be valid or not based on simultaneous line-end extensions and design rule checks for M2 and via layers. Thus, the hit point combination in Fig. 6 (d) is valid as a legal set of M2 and via patterns can be obtained to access this particular standard cell. All possible hit point combinations can be enumerated

based on backtracking scheme [64], which generates a compact set of valid hit point combinations. For standard cell designers, a robust standard cell shall provide maximized number of valid hit point combinations, which can be quickly evaluated by the pin access optimization and evaluation engine aforementioned. Moreover, standard cells are placed next to each other instead of being isolated in real designs. This means both intra-cell and inter-cell pin accessibility shall be evaluated and optimized before the routing stage [68], [69]. In our experiments on ARM 10 nm predictive standard cell library, compared with conventional design rule check (DRC), we achieve 10X or more improvement for most cells and some cells achieve up to a 10,000X increase in the number of valid hit point combinations [63].

4. Pin Access and Routing Co-Optimization

In advanced technology nodes, standard cell architecture limits the number of routing tracks available for net connections, which induces high routing density and severe routing resource competition, namely standard cell pin access issue [21]. Standard cell designers can address this issue by I/O pin optimization with the assistance from pin access optimization and evaluation engine [63], [72]. A detailed placement engine can mitigate routing resource competitions by intelligent cell spreading [58]. Global routing can benefit routing closure by accurate modeling of local pin access impact on routing resources. However, for a given design with cell placement, the detailed router still takes the full responsibility for routing closure by resolving routing resource competitions and finishing all net connections [47], [50], [68], [69]. In this section, we first discuss routing-level pin access interference, which will be tackled by pin access planning and routing interval generation and assignment schemes. We further discuss how to incorporate these schemes into a negotiation-congestion-based routing framework.

4.1 Pin Access Interference

In the routing level, pin access interference is an outcome of routing resource competitions among I/O pins close to each other [63]. For clear descriptions of pin access interference, we present the following definition.

Definition 3 (Pin Access Routing Interval) *A pin access routing interval is defined as a segment of unidirectional M2 pattern connected to an I/O pin on a specific routing track.*

As an example, pin access interference on M2 is illustrated in **Fig. 7**, where there exist 5 pins including a_1, b_1, c_1, c_2 and d_1. Pin c_1 and c_2 belong to the same net and need to be connected with M2 routing patterns. One way to access these pins is shown in Fig. 7 (a), which leads to pin access failure because pin c_1 is blocked by existing pin access routing intervals. The main task of pin access and routing co-optimization is to obtain pin access success as shown in Fig. 7 (b), where a different set of pin access routing intervals is selected for net connections. Therefore, an advanced detailed router should be able to resolve pin access interference efficiently for unidirectional routing closure.

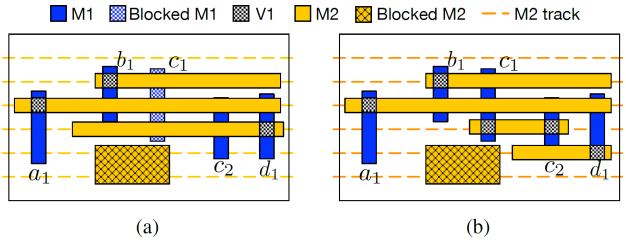

Fig. 7 Pin access interference on M2, (a) pin access failure, (b) pin access success [68].

4.2 Pin Access Planning

To date, manufacturing-friendly detailed routing studies follow the paradigms of sequential routing [11], [13], [28], [37], [45], [46] and negotiation-congestion-based routing technique [8], [9]. When a router accesses an I/O pin locally, it creates a routing interval pattern on M2 for the net connection as shown in Fig. 7. With unidirectional routing style, the physical location of that particular pin access routing interval, including routing track and left/right edge position, depends on underlying path-finding algorithm, which typically focuses on routing cost minimization without leveraging the overall standard cell pin accessibility. This means pin access routing intervals for routed nets could damage the pin accessibility of I/O pins associated with remaining nets as illustrated in Fig. 7 (a), i.e., pin access interference.

For better routing closure, it is important to create meaningful planning schemes for a sequential router and leverage the overall pin accessibility during a sequential routing procedure, which is the major focus of local and global pin access planning schemes [68], [69]. For single-net routing, the key to local pin access planning is dynamic hit point scoring. We assign a score to each hit point of an I/O pin based on the number of available hit point combinations for that particular hit point, which changes dynamically when pin access routing intervals are created for other net connections. When a router accesses the pin locally, the router is forced to take the hit point with the highest score, which implies the best pin accessibility for remaining I/O pins for that particular standard cell. During sequential routing process, routed wires on M2 layer are created on top the I/O pins for remaining nets as shown in **Fig. 8**. This makes the order of net routing particularly important for pin access interference among

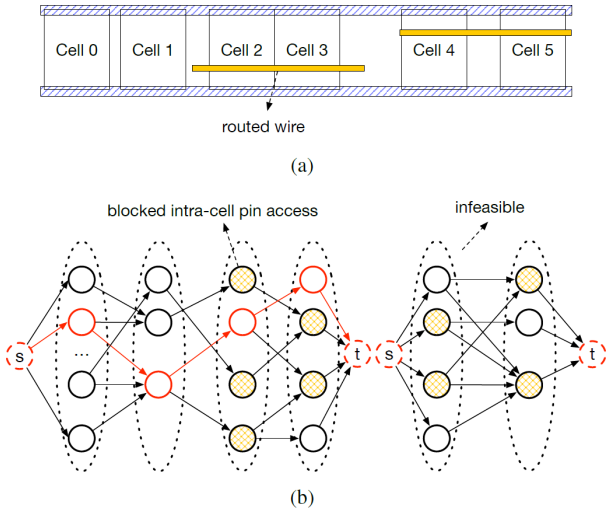

Fig. 8 Single row pin access graph (PAG), (a) cell placement, (b) simplified PAG with routed wires [68], [69].

all nets. Net deferring technique has been proposed to dynamically change the order of net routing, which globally preserves the pin accessibility of I/O pins for remaining nets. This scheme depends on the single row pin access graph (PAG) to determine whether a net will be deferred or not during sequential routing procedure [68], [69].

An example of single row PAG is shown in Fig. 8 (b), where corresponding standard cell placement and routed M2 wires are illustrated in Fig. 8 (a) [69]. Each component in the single row PAG is a directed graph from source (s) node to target (t) node, where each internal node in Fig. 8 (b) corresponds to a valid hit point combination for a specific cell in Fig. 8 (a). An edge is added from left node to right node if associated hit point combinations for neighboring cells are compatible with each other. For the PAG, we have following observation [69].

Observation 1 *The pin accessibility of the standard cells on the M2 layer within the single row is equivalent to the existence of a path from s to t of the PAG associated with that particular row. We define a PAG component to be infeasible for pin access when no feasible path exists from s to t of that PAG component.*

The PAGs are dynamically updated during sequential routing. When one component of the PAGs has no path from source to sink, the net being routed will be deferred, which means routed wires will be cleared and the net will be put back to the priority queue with an updated priority. The local and global pin access planning schemes can guide a sequential router for better pin accessibility and unidirectional routing closure [68], [69].

4.3 Routing Interval Generation and Assignment

With pin access planning schemes, it is still difficult for a sequential router to achieve routing closure without significant engineering-changing-efforts [68], [69]. Negotiation-congestion-based routing scheme outperforms general sequential routing approaches because history cost is introduced to resolve the net congestions in an efficient manner [43]. However, high routing densities and severe routing resource competitions on lower metal layers cause significant routing overhead for the router. An alternative to reduce routing overhead is to design and optimize pin access routing intervals concurrently for all I/O pins, which are fed into the router for better routing closure [1], [50]. The routing interval generation and assignment approach resolves the routing resource competitions among I/O pins on lower metal layers concurrently before the routing phase starts. When a router takes optimized pin access routing intervals for I/O pins as an input, each I/O pin has assigned a pin access routing interval and routing resource competitions have been resolved, which significantly reduces the net congestions during a routing procedure.

To resolve pin access interference, Ref. [47] proposes pin access path pre-computation and optimization for gridless routing, but it cannot be directly applied in advanced technology nodes due to the unidirectional routing style. RegularRoute [80] proposes a terminal promotion heuristic to access standard cell I/O pins, which could lead to inefficient usage of routing resources on lower metal layers. The detailed routing study for dense pin clusters [50] proposes an insightful solution in terms of escape routing to obtain a set of pin access routing intervals on a specific metal layer. The escape routing of I/O pin clusters is formulated as a multi-commodity flow problem and solved with efficient Lagrangian relaxation algorithm. In advanced technology nodes, this problem becomes more challenging due to high routing density and advanced manufacturing constraints. Without delivering details on the routing interval generation, BonnRoute further generalizes the maximum weighted independent set algorithm to compute routing interval assignment for each I/O pin with maximum profits [1].

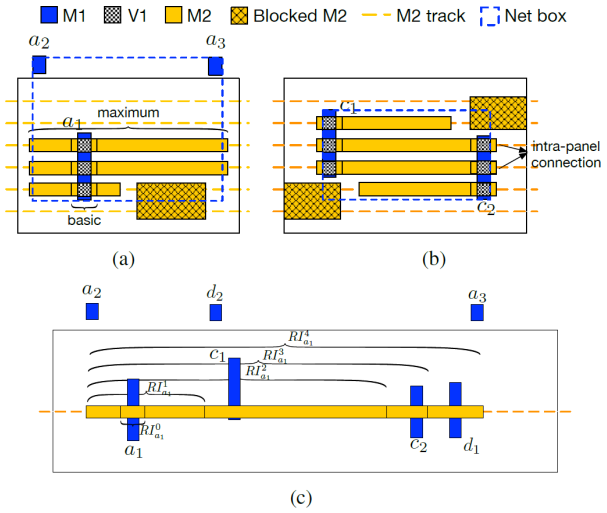

Fig. 9 Routing interval generation, (a) a pin close to M2 blockages, (b) two pins sharing the same net, (c) handling pin-to-pin interference.

Our recent routing study provides novel solutions for both routing interval generation and assignment. An example of track-based routing interval generation is illustrated in **Fig. 9**. As shown in Fig. 9 (a), we generate candidate routing intervals for each I/O pin according to net bounding box (net box), routing tracks and blockages. A basic routing interval is a minimum-sized routing pattern over an I/O pin, while a maximum routing interval spans over the entire net box horizontally, which denotes the maximum M2 usage for the net connecting a_1, a_2 and a_3 without detour. Figure 9 (b) demonstrates the candidate routing interval generation for pin c_1 and c_2 sharing the same net. The routing intervals enabling intra-panel net connections shall be favored during the routing interval assignment phase because they provide optimal routing patterns for that particular net. Figure 9 (c) illustrates a general example for pin a_1 considering pin-to-pin interference, which includes 5 routing intervals ($RI^0_{a_1}$ to $RI^4_{a_1}$) for pin a_1. With routing interval candidates generated for each I/O pin, the following step is to resolve the conflicts among routing intervals while selecting one routing interval for each I/O pin with maximized profits. In general, routing interval generation and assignment problem can be formulated as an integer linear programming problem. Taking advantage of the uniqueness of this formulation, we further propose an iterative greedy algorithm based on the Lagrangian relaxation technique for scalable solutions.

4.4 Manufacturing-Friendly Unidirectional Routing

Most existing manufacturing-friendly studies focus on the coloring scheme of routing patterns while leveraging SAMP-specific manufacturing constraints [8], [9], [11], [13], [28], [37], [45],

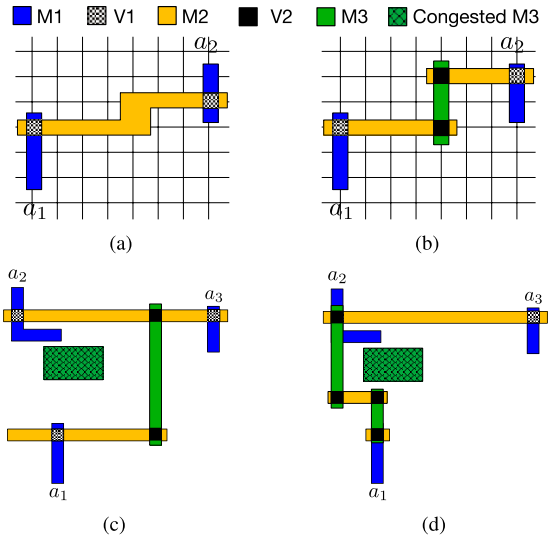

Fig. 10 (a) Two-dimensional routing, (b) unidirectional routing, (c) more wirelength with routing interval assignment, (d) more vias without routing interval assignment.

[46], [57], [68]. Reference [45] presents the first SADP-aware detailed routing study by considering SADP-specific constraints during sequential routing procedure. Reference [13] further improves the routing results by incorporating coloring scheme and layer assignment into a sequential router. Refereces [28], [29] focus on novel grid coloring techniques to guarantee SADP and SAQP friendliness during routing. Reference [9] proposes a novel graph model to capture the SADP-specific manufacturing constraints and delivers SADP-friendly routing results with negotiation-congestion-based routing scheme. References [37] and [8] further enhance the graph model for better results by considering overlay constraints and via model, respectively. These studies aforementioned rely on two-dimensional patterns, which contradicts with the pure unidirectional routing style in advanced technology nodes.

Although unidirectional routing style reduces the routing solution space compared to routing with two-dimensional patterns, it provides valuable opportunities to efficiently resolve routing resource competitions and trim/cut mask constraints during routing. **Figure 10** (a) and (b) demonstrate the single-net routing patterns for two-dimensional routing and unidirectional routing, respectively. For two-dimensional routing, routing patterns orthogonal to the preferred direction of a metal layer will be much thicker than regular metal patterns to improve the manufacturability and a router typically selects hit points for I/O pins based on wirelength minimization for the net connection. While for unidirectional routing, switching routing direction means changing routing layers, which potentially introduces more vias and larger wirelength. With unidirectional routing style, Ref. [11] presents a track assignment approach to handling the cut mask complexities efficiently. Reference [57] proposes global routing studies to reduce cut mask complexities for SAMP-aware routing. Reference [68] introduces local and global pin access planning schemes for better unidirectional routing closure, which generates superior routing results compared to a two-dimensional SADP-friendly router [37].

Moreover, unidirectional routing style ratifies the phase of routing interval generation and assignment before the detailed routing stage. An example of single-net routing is shown in Fig. 10 (c) and Fig. 10 (d) for detailed routing results with and without routing interval assignment, respectively. With routing interval assignment, fewer turns will be created by the router, which generates fewer vias at the cost of some detour as shown in Fig. 10 (c). Without routing interval assignment, the router delivers routing patterns with minimized overall cost, which typically leads to close-to-optimal wirelength as shown in Fig. 10 (d). Despite wirelength overhead, our recent routing study demonstrates that, by incorporating the results from routing interval generation and assignment, a negotiation-congestion-based router can obtain much better routing results, i.e., unidirectional routing closure, than state-of-the-art manufacturing-friendly routing studies [8], [68]. Specifically, compared to sequential routing with pin access planning schemes [68], our proposed approach obtains over 15% wirelength reduction and over 10X runtime speed-up. Compared to a pure negotiation-congestion-based routing scheme without routing interval generation and assignment [8], our approach achieves over 14% via number reduction and over 2X runtime speed-up.

5. Post-Routing Optimization

In advanced technology nodes, unidirectional line patterns can be manufactured with tight overlay control using self-aligned type of MPL [16], [56]. To obtain target routing patterns, manufacturing-friendly cut/trim mask is designed to remove undesired portions of the lines as illustrated in Fig. 2 (c) and Fig. 2 (d). A detailed router is able to follow a specific set of manufacturing constraints in the routing procedure or based on additional rip-up and reroute [8], [69]. However, design rule violations may still exist after the routing phase, which makes post-routing optimization very important for the unidirectional routing closure in advanced technology nodes. Moreover, yield enhancement with wiring and via redundancy has been widely adopted in industry, which remains an important option for post-routing optimization in advanced technology nodes. In this section, we first present the full-chip redundant local loop insertion compatible with unidirectional routing style. Then, cut/trim redistribution techniques are discussed with various lithography options, which targets at final unidirectional routing closure.

5.1 Redundant Local-Loop Insertion

During the layout manufacturing process, via and wiring failures are major causes for the yield loss [4]. Therefore, redundant via [31], [41] and redundant wire [5], [26] insertions have been proposed to improve manufacturing yield. However, traditional redundant via insertion is not compatible with unidirectional routing style as shown in **Fig. 11** (a). Conventional redundant via insertion assumes wire bending for the metal coverage of redundant vias to be inserted, which conflicts with the unidirectional routing style. As shown in Fig. 11 (b), a redundant local loop can be adopted to insert redundant vias and wires simultaneously to enhance the yield of unidirectional routing [4].

The concept of redundant local loop is first proposed in Refs. [2], [4]. Reference [22] further quantifies the yield and

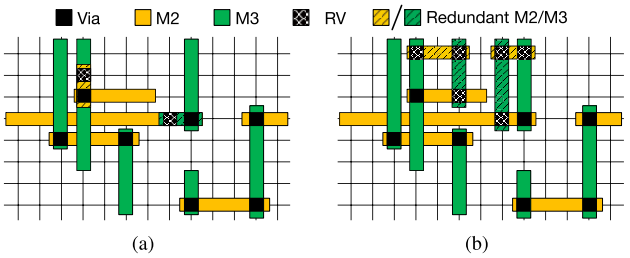

Fig. 11 (a) Redundant via insertion with wire bending, (b) redundant local loop insertion for unidirectional routing [67].

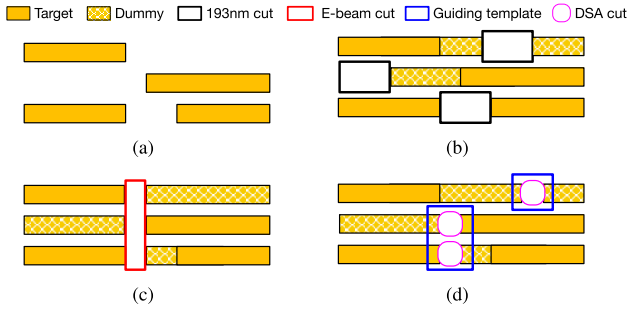

Fig. 12 Post-routing decomposition with line-end extensions, (a) target patterns, (b) 193 nm cut [16], [56], (c) E-beam cut [7], [10], (d) guiding template with DSA cut [61].

timing impact from redundant local loop insertions. The timing degradations from redundant local loop insertion are demonstrated to be negligible [22]. Early studies on redundant local loop insertion focus on greedy insertion schemes without giving globally optimized solutions. Our recent study proposes a full-chip redundant local loop insertion engine with net-based redundant local loop candidate generation while accommodating self-aligned via [53] and via density constraints [25], [32]. Instead of adopting a simple greedy scheme [2], [4], [22], we further propose an optimal integer linear programming formulation and a scalable iterative relaxation and linear programming solving scheme to obtain much better results in terms of insertion rate and overall cost. Our study also revisits the timing impact of redundant local loop insertion with delay model analysis and timing simulations. We find that specific configurations of the redundant local loop can introduce significant timing degradations in a predictive 10 nm technology setup. Thus, these local-loop configurations should be strictly forbidden during redundant local loop insertion for negligible timing impact.

5.2 Cut/Trim Mask Redistribution

Although unidirectional routing patterns simplify the coloring schemes of MPL, manufacturing complexities arise in the manufacturing-friendly cut/trim mask designs. As illustrated in Fig. 2 and Fig. 3 (a), the line-end positions of unidirectional routing patterns decide the shapes and positions of cut/trim masks. If we assume single patterning with 193 nm lithography tools for cut/trim mask, a set of SADP-specific line-end rules can be determined for routing patterns to generate lithography-friendly cut/trim masks as shown in Fig. 3 (a) [63]. A detailed router can be required to follow a set of metal and via design rules during routing procedures. However, design rule violations may still exist after the routing phase due to problem complexities and runtime. Therefore, line-end extensions, i.e. allowing dummy patterns, have been widely used to enable manufacturing-friendly cut/trim mask designs as shown in **Fig. 12**.

References [78], [79] present early studies on manufacturability improvement of cut masks with line-end extensions, where a greedy approach is used to redistribute cut shapes for better printability. A mixed integer linear programming formulation is presented in Refs. [63], [64] to obtain SADP-friendly pin access patterns with minimum amount of line-end extensions. For unidirectional layout with cut/trim mask, emerging lithography techniques can be further deployed, such as LELE, E-beam and DSA, to improve density and spacing of cut/trim masks. As shown in Fig. 12 (b), line-end extensions can be performed to enable cut merging and E-beam-friendly cut shapes, which provides much better tip-to-tip control compared to single patterning [7], [10]. Recently, DSA has been shown as a promising lithography candidate to print small layout patterns. Meanwhile, DSA brings unique lithography constraints into layout design stage, where a set of 193 nm lithography-friendly guiding templates needs to be designed first before printing smaller DSA cuts. With guiding template constraints, DSA has been adopted for cut mask design and line-end extensions with a greedy scheme [61]. Mixed integer linear programming formulations and dynamic programming algorithms have been proposed to enable DSA-friendly cut mask designs [35], [36], [48], [49]. Given a set of design rules, line-end extension problems aforementioned are similar to the layout migration issue [20], where the objective is to minimize the amount of dummy patterns and the design rules are formulated as linear constraints. The (mixed integer) linear programming based line-end extensions can help to obtain lithography-friendly layout, which greatly reduces the amount of engineering-changing-efforts for routing closure.

6. Conclusion and Future Direction

In this paper, we present a holistic approach to enable unidirectional routing closure on lower metal layers in advanced technology nodes. A standard cell pin accessibility evaluation and optimization engine is presented to guide standard cell designers for incremental cell layout optimization. Pin access planning schemes and routing interval generation and assignment techniques are discussed to efficiently resolve the pin access interference for a sequential router and a negotiation-congestion-based router, respectively. In the post-routing stage, redundant local loop insertion and cut/trim mask redistribution are comprehensively discussed to improve manufacturing yield and enable layout design closure under advanced manufacturing constraints, respectively.

Unidirectional routing style is becoming the mainstream industrial routine for high-density metal layers in advanced technology nodes. For better routing closure and overall physical design closure, we anticipate more and more research efforts in this direction from following perspectives.

- Generic standard cell library evaluation tool. Hit points and hit point combinations are elementary metrics for pin accessibility evaluation and optimization. For manual design

and optimization, a generic scoring function is favorable while considering pin accessibility, colorability [65], [66] and manufacturing-specific design rules.

- Placement mitigation. The complexities of cell coloring, inter-cell pin accessibility and other manufacturing constraints interfere with each other, which makes it difficult to predict the appropriate spacing among standard cells [19], [58]. Advanced placement engine is needed to properly allocate white space among standard cells for better design closure.
- Concurrent multi-layer detailed routing. Routing interval generation and assignment can only resolve routing resource competitions on one metal layer. It remains an open research problem of how to enable concurrent multi-layer detailed routing beyond negotiation-congestion-based routing without significant wirelength or runtime overhead [23].
- Global and detailed routing co-optimization. Most existing manufacturing-friendly routing studies focus on detailed routing phase as detailed router creates real physical patterns, which are directly associated with manufacturing constraints. However, this is no longer an effective approach when the routing resource competitions are severe and many local nets cannot be routed due to inaccurate routing resource modeling for global routing, which requires global and detailed routing co-optimization.

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