Overlay Aware Interconnect and Timing Variation Modeling for Double Patterning Technology

Jae-Seok Yang, David Z. Pan
Dept. of ECE, The University of Texas at Austin, Austin, Tx 78712
jsyang@cerc.utexas.edu, dpan@ece.utexas.edu

***Abstract*— As Double Patterning Technology (DPT) becomes the only solution for 32-nm lithography process, we need to investigate how DPT affects the performance of a chip. In this paper, we present an efficient modeling of timing variation with overlay which is inevitable for DPT. Our work makes it possible to analyze timing with overlay variables. Since the variation of metal space caused by overlay results in coupling capacitance variation, we first model metal spacing variation with individual overlay sources. Then, all overlay sources are considered to determine the worst timing with coupling capacitance variation. Non-parallel pattern caused by overlay is converted to parallel one with equivalent spacing having the same delay to be applicable of a traditional RC extraction flow. To verify our work, we use identical interconnects having different positions and different layout decompositions. Experimental result shows that the delay has a variation from 7.8% to 9.1% depending on their locations. The well decomposed structure shows only 2.7% delay variation.**

I. Introduction

As the minimum pitch size decreases, the lithography process has been confronted with severe limitation. The traditional lithography using 193nm wavelength light cannot print sub-32nm pattern. The smallest feature size to be printed is defined as K1·λ/NA in which K1 is referred to as K-factor for a given process, λ is a wavelength of a light source, and NA is a numerical aperture determined by lens size. When we use immersion lithography of NA=1.2, K-factor should be less than 0.2 to print 32nm pattern. However, the theoretical limitation of K-factor is 0.25 with intensive OPC [1].

Another solution for 32nm patterning is to use a strong light source. EUV is a promising candidate for a light source of future lithography equipment. Since the wavelength of EUV light source is 13.5nm, theoretically, EUV lithography can make sub-10nm pattern. However, it is not clear when EUV equipment will be commercially available because of the difficulty in dealing with the strong light source. The alternative technology for 32nm technology is Double Patterning Technology (DPT). Since DPT does patterning twice, we can print two lines in a pitch which reduces K-factor to 0.125. Even though DPT is an inefficient process because of the low throughput, the industry is trying to adopt DPT as a solution of 32nm patterning because DPT is probably the only technology to be available before EUV equipment is shipped.

The difficulty of DPT is the stitch generation and overlay control to reduce mask misalignment between the first and second lithography steps. The advanced lithography equipment has about 5nm of overlay in 3-σ level which is relatively large compared with 32nm half pitch size [2], [3]. Since overlay may change the circuit behavior such as timing, noise, and power due to the distortion of layout pattern, we need a methodology to estimate the variation due to overlay during design. Metal layer variation due to overlay can affect the circuit performance and yield seriously because overlay changes coupling capacitance between metals.

In this paper, we present a systematic method to estimate the performance variation with several overlay variables. This is the first work to deal with overlay and timing relation, to our best knowledge. From the overlay measurement, it is possible to distinguish sources of overlay which are translation, rotation, and magnification. Since overlay changes metal spacing, we model coupling capacitance to be a function of overlay variables. Metal spacing with overlay is not constant because overlay effects are different on a position by position. Thus, parallel interconnects become non-parallel after overlay modeling. To be able to use traditional 2.5-D extraction tool, non-parallel conductors are converted to parallel layers with equivalent spacing in terms of timing behavior. After modeling capacitance with overlay variables, we show how to analyze timing by sweeping overlay variables, and determine the variables which make the worst timing. With these variables, we can construct a new equivalent layout with overlay consideration for an effective timing analysis.

The contributions of this paper include the following:

- This paper provides a set of analytical formulae to model coupling capacitance variation induced by overlay.
- This paper shows that the timing variation due to overlay can be up to 9.1% at 32nm technology.
- This paper also shows that layout decomposition methods [4], [5] play a role in timing variation reduction.

The rest of the paper is organized as follows. The background knowledge is presented in section II. We propose how to model timing variation in section III. The determination of overlay variables to make the worst timing is presented in section IV. In section V, the application of the work and experimental results are shown. We conclude in section VI.

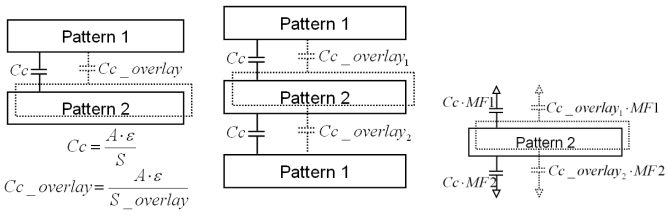
II. Background

A. Capacitance variation induced by overlay

Since coupling capacitance is inversely proportional to spacing between two conductors, a spacing variation due to overlay

This work is supported in part by NSF, SRC, and Samsung Scholarship.

978-1-4244-2820-5/08/$25.00 ©2008 IEEE

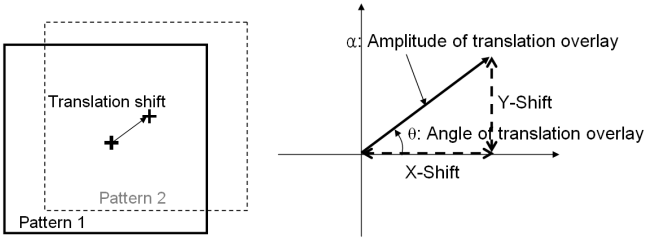


(a) One sided cap. (b) Two sided cap. (c) Decoupled cap.

Fig. 1. Effective capacitance variation.

in DPT results in a variation of a coupling capacitance [6]. For instance, if metal spacing without overlay is 50nm and overlay reduces the spacing by 10nm, Cc_overlay is equal to 1.25Cc in Figure 1(a). One sided capacitance variation is understood explicitly. Overlay effect in Figure 1(b) is not clear because the total capacitance is changed from 2Cc to 2.08Cc (Cc_overlay1: 1.25Cc, Cc_overlay2: 0.83Cc) at spacing=50nm, Y-translation overlay=10nm. However, if interconnects have different slew rate, we can see clearly overlay effect on timing. The coupling capacitance can be substituted to an equivalent grounded capacitance for an equal delay [7], [8]. The miller factor is defined as MF = 1 + Tv/Ta. Here, Tv is a transition time of victim, and Ta is a transition time of aggressor. If MF1 is three, and MF2 is one in Figure 1(c), the total decoupled capacitance is 4.58Cc which is 14.5% bigger than the capacitance (4Cc) in case of ignoring overlay. From this observation, overlay in DPT has a significant effect on an effective capacitance for multiple aggressor case as well as single aggressor case.

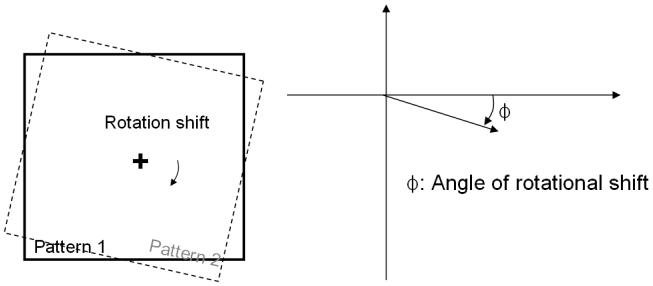
B. Sources of overlay



(a) Translation overlay (b) Variables for translation overlay

Fig. 2. Translation overlay variable.

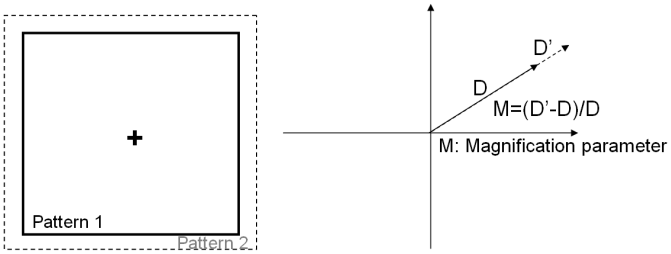
In this paper, overlay variables are assumed to be measured from the misalignment between the first and the second patterning. For simplicity, we assume that overlay is a systematic variation, and randomly generated overlay is negligible. There are three types of overlay [9]. The first one is a translation overlay which is caused by mismatching a mask in a horizontal or vertical direction. The translation overlay has two variables. The first variable is overlay amplitude. The amplitude in advanced lithography system is in the range of 3nm to 5nm. From a wafer measurement, we can extract the overlay amplitude of 3-σ level. The second variable is overlay angle which is purely random because a translation shift can be any direction. In this paper, overlay amplitude will be symbolized as α, and overlay angle is expressed as θ in Figure 2. The counterclockwise of θ is defined as a positive θ.



(a) Rotation overlay (b) Variable for rotation overlay

Fig. 3. Rotation overlay variable.

The second source of overlay is a rotation of masks between the first patterning and the second patterning. Even though the rotation overlay is less than 0.1μ radian in advanced equipment, rotation overlay can make several nm of layout distortion at the edge of a die. A variable of rotation overlay is ϕ, and the clockwise direction of rotation is defined as positive ϕ as shown in Figure 3. Rotation overlay depends on pattering location and the amount of ϕ.



(a) Magnification overlay (b) Variable for magnification overlay

Fig. 4. Magnification overlay variable.

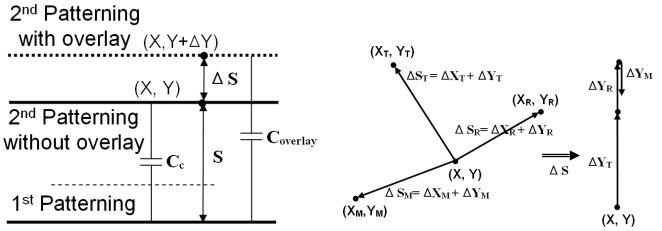
The last component of overlay is called magnification overlay. If there is a temperature variation between the first and the second lithography step, there is magnification overlay because a mask has a different thermal expansion rate with a wafer. In a projection lithography system, a magnification factor fluctuation is another source of magnification overlay. The variation on layout due to magnification overlay is bigger as the pattern is far from the center point. A variable of magnification overlay is defined to M in Figure 4. A positive M means the second patterning is enlarged than the first one. M is less than 0.1ppm in an advanced lithography equipment. The overlay variables are extracted in 3-σ level from overlay measurement [9].

III. Layout distortion estimation

We will propose a numerical formula to predict coupling capacitance variation induced by overlay in this section.

A. Problem definition

In Figure 5(a), C_C is a coupling capacitance obtained by standard RC extraction tool without overlay consideration. $C_{overlay}$ is a coupling capacitance with overlay modeling. (X, Y) is a node on 2^{nd} patterned interconnect. The original space(S) is increased by ΔS which makes C_C to be $C_{overlay}$. Each overlay source makes a shift of (X,Y). (X, Y) is shifted to (X_T, Y_T) by translation overlay. (X_R,Y_R) is a shifted point



(a) $C_{overlay}$ definition (b) ΔS definition

Fig. 5. Vector expression of overlay.

by rotation overlay. Similarly, (X,Y) moves to (X_M,Y_M) by magnification overlay. The overall shift is the sum of each movement.

$$\Delta S = \Delta S_T + \Delta S_R + \Delta S_M \tag{1}$$

Since two metals are parallel horizontally, ΔS is equal to ΔY. In Figure 5(b), metal space is increased by ΔY_T+ΔY_R+ΔY_M. Since coupling capacitance is in inverse proportional to metal space, $C_{overlay}$ is a function of ΔS in the following.

$$C_{overlay} = \frac{S}{S + \Delta S} \cdot C_C \tag{2}$$

To incorporate overlay measurement, we need a formula of ΔS with overlay variables.

B. Translation overlay consideration

To predict metal space for translation overlay, let us assume that (X,Y) is moved to (X_T, Y_T) by α and θ.

$$(X, Y) \overset{\alpha,\theta}{\leftrightarrow} (X_T, Y_T) \tag{3}$$

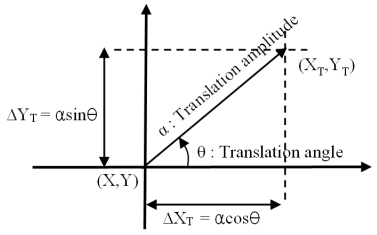


Fig. 6. ΔX_T and ΔY_T for translation overlay.

From Figure 6, X-translation(ΔX_T) is $\alpha cos\theta$, and Y-translation(ΔY_T) is $\alpha sin\theta$. Even though ΔX_T and ΔY_T depend on α and θ, ΔS_T is not proportional to α and θ directly because ΔS_T depends on a geometric relation.

Figure 7 shows possible geometric relations which are represented by γ defined as a degree between X-axis and orthogonal vector from 1^{st} pattern to 2^{nd} pattern. Since metal space is changed by X-translation overlay when two metals are parallel in vertical direction, ΔS_T is equal to ΔX_T for γ=0. Similarly, ΔS_T is ΔY_T for γ=π/2. We calculate ΔS_T for every geometric relation in Figure 7. ΔS_T is generalized in the following equation.

$$\Delta S_T = \alpha \cdot cos\,(\theta - \gamma) \tag{4}$$

Equation 4 makes us consider a capacitance variation with translation overlay. Since γ represents geometric relations, it

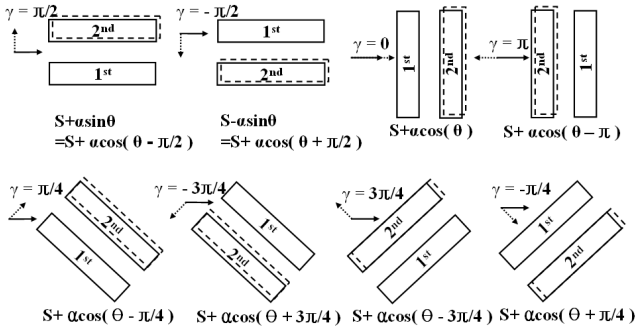


Fig. 7. ΔS_T for various geometric relations.

is a fixed value for a given decomposed layout. Thus, it is possible to analyze a timing variation with θ and α variables.

C. Rotation overlay consideration

To predict metal space for rotation overlay, let us assume that (X,Y) is moved to (X_R,X_R) by ϕ rotation.

$$(X, Y) \overset{\phi}{\leftrightarrow} (X_R, Y_R) \tag{5}$$

Since the effects of rotation overlay are not the same when their positions are different, we need to consider locations of patterns for estimating distortion induced by rotation overlay.

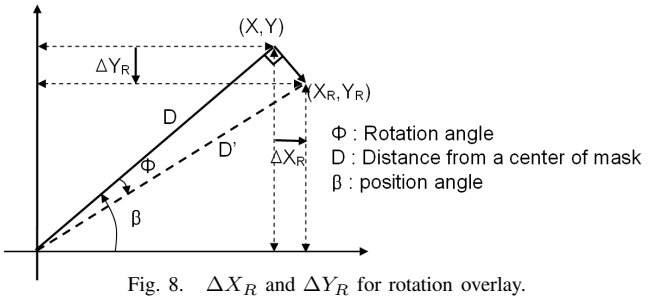


Fig. 8. ΔX_R and ΔY_R for rotation overlay.

The location of (X,Y) is expressed by the distance(D) from the center and the angle(β) from X-axis in Figure 8. D' is a distance from the center to (X_R, Y_R). β is a position angle which is positive in a counterclockwise.

$$D = \sqrt{X^2 + Y^2}, D' = D/\cos\phi \tag{6}$$

ΔX_R with ϕ rotation is $|X_R - X|$, and ΔY_R is $|Y_R - Y|$. ΔX_R and ΔY_R are obtained from Figure 8.

$$\begin{aligned} \Delta X_R &= D \cdot \{\cos(\beta - \phi) / \cos\phi - cos\beta\} \\ \Delta Y_R &= D \cdot \left\{\cos\left(\beta + \frac{\pi}{2} - \phi\right) / \cos\phi - cos\left(\beta + \frac{\pi}{2}\right)\right\} \end{aligned} \tag{7}$$

ΔX_R and ΔY_R have $\pi/2$ phase difference which is useful for deriving a general formula.

$$\Delta S_R = D \cdot \{\cos(\beta' - \phi) / \cos\phi - cos(\beta')\} \tag{8}$$

In equation 8, β' is a new variable considering both geometric relation and position angle. When the geometric relation is γ=0, metal space is increased by ΔX_R. Thus, β' is equal to β when γ is zero. If γ is π, ΔS_R is -ΔX_R because

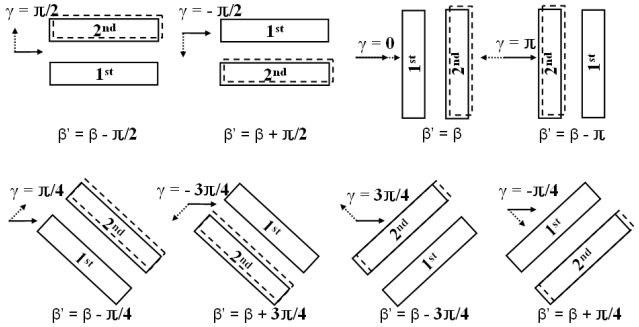


Fig. 9. β' for various geometric relations.

metal space decreases for the relation. Since π phase shift of cos changes its sign, β' is β-π when γ is π. Similarly, we calculate β' for every relation in Figure 9. General formula of ΔS_R is in the following equation.

$$\Delta S_R = D \cdot \{\cos(\beta - \gamma - \phi) / \cos\phi - \cos(\beta - \gamma)\} \quad (9)$$

We can model a capacitance variation with rotation overlay using equation 9. D and β is determined by initial position (X,Y). Since γ is a fixed value for a given decomposed layout and ϕ is only a variable, we can analyze a timing variation by sweeping the rotation variable from -ϕ to +ϕ.

D. Magnification overlay consideration

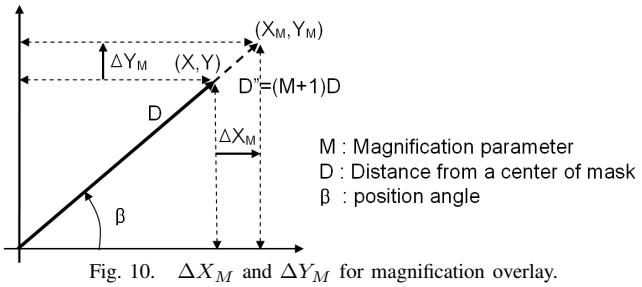


Fig. 10. ΔX_M and ΔY_M for magnification overlay.

D" is defined as a distance from the center to a shifted point due to magnification overlay. Since M is defined as (D"-D)/D, D"-D is equal to M·D. Thus, ΔX_M and ΔY_M are obtained in the following.

$$\Delta X_M = M \cdot D \cdot cos\beta, \Delta Y_M = M \cdot D \cdot sin\beta \quad (10)$$

The layout distortion due to magnification overlay is generalized in the following.

$$\Delta S_M = M \cdot D \cdot cos(\beta - \gamma) \quad (11)$$

Since M is only a variable in DPT in Equation 11, we can analyze timing variation by sweeping the magnification variable from -M to +M.

E. Overall capacitance variation with overlay

$$\begin{aligned}\Delta S &= \Delta S_T + \Delta S_R + \Delta S_M \\ &= \alpha \cdot cos(\theta - \gamma) \\ &+ D \cdot \{\cos(\beta - \gamma - \phi) / \cos\phi - \cos(\beta - \gamma)\} \\ &+ M \cdot D \cdot cos(\beta - \gamma)\end{aligned} \quad (12)$$

In equation 12, we propose the numerical expression of ΔS parameterized by overlay variables, location, and geometric relation. Even though rotation and magnification overlay depend on their initial position, the linear summation of each spacing variation gives us an accurate result. We will show that initial point change due to other overlay source is negligible in section IV.

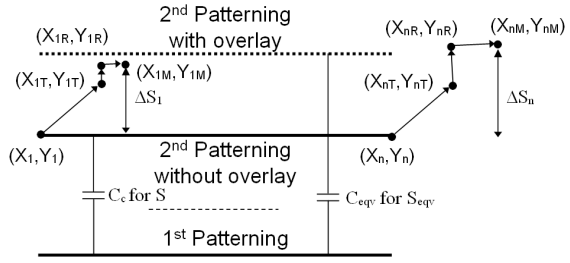


Fig. 11. ΔS dependency on location.

Non-parallel metal layer after overlay consideration should be converted to parallel one with equivalent timing behavior to be applicable of 2.5D RC-extractor which cannot deal with a diagonal pattern. In Figure 11, we assume that (X_1,Y_1) is close to a driver, and (X_n,Y_n) is close to a receiver. ΔS_1 is a metal spacing variation at (X_1,Y_1) while ΔS_n is metal spacing variation at (X_n,Y_n). ΔS_T is the same in every position of a die because ΔS_T is independent of a location. However, since ΔS_R and ΔS_M depend on their initial position, ΔS_1 is different with ΔS_n.

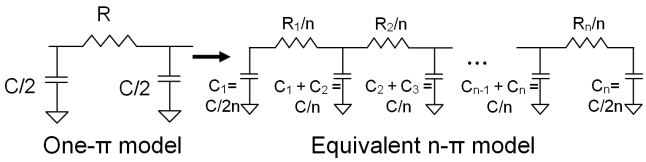


Fig. 12. Equivalent n-π model for S_{eqv} calculation.

S_{eqv} is defined as the metal spacing to have an equivalent delay. To find S_{eqv}, interconnect is assumed to be modeled by n-π model which is equivalent to one-π model in Figure 12. C_i and R_i is the capacitance and resistance in i^{th}-π structure. The capacitance at the driver is C_1, and the one at the receiver is C_n.

$$\frac{R}{2n}\left\{\sum_{i=1}^{n-1}\frac{i}{n}(C_i + C_{i+1}) + C_n\right\} \quad (13)$$

Using elmore delay model, the delay of n-π model is expressed in equation 13. When C_1 is equal to C_n, the above equation becomes $R \cdot C/2$ which is the same value with the delay of one-π model. When C_1 is not equal to C_n, the delay of interconnect is $R{\cdot}C_{eqv}/2$ because the resistance is constant. C_{eqv} is the equivalent capacitance after converting to parallel pattern.

$$\begin{aligned}\Delta C &= C_{i+1} - C_i = \frac{C_n - C_1}{n-1} \\ C_i &= C_1 + \Delta C \cdot (i-1) \\ C_{i+1} &= C_1 + \Delta C \cdot i\end{aligned} \quad (14)$$

ΔC is a step increase of capacitance for n-π model. Equation 13 can be expressed by C_1 and ΔC. As n goes infinite, the delay of interconnect is presented in the following.

$$\lim_{n\to\infty}\left[\frac{R}{2n}\left\{\sum_{i=1}^{n-1}\frac{i}{n}(2C_1-\Delta C+2\cdot\Delta C\cdot i)+C_n\right\}\right] \quad (15)$$

After simplifying, equation 15 becomes R·C_1+2C_n/6 which should be equal to R·C_{eqv}/2.

$$C_{eqv}=\frac{1}{3}\cdot C_1+\frac{2}{3}\cdot C_n$$
$$S_{eqv}=\frac{3\cdot S_1\cdot S_n}{2\cdot S_1+S_n} \quad (16)$$

Here, S_1 is S+ΔS_1, and S_n is S+ΔS_n. Since there is a resistance shield effect, the capacitance close to a receiver has more effect on delay, and equation 16 implicates the physical meaning.

$$C_{overlay}=\frac{S}{S_{eqv}}\cdot C_C \quad (17)$$

Every coupling capacitance can be represented by equation 17 after overlay consideration.

IV. Timing analysis with the parameterized capacitance

This section will show the determination of overlay variables to be the worst timing result. Once we decide the variables for the worst delay, we can modify a layout with overlay variables that is able to be used for the worst corner timing simulation. Then, the traditional timing analysis flow can be used for the layout which is modified to maximize the delay with overlay. There are four overlay variables defined in this paper. Obviously, the large values of variables maximize the distortion of layout. However, ϕ and M are a signed value, and the angle of translation overlay is purely random variable. Thus, the efficient way of determining ϕ, M and θ for the worst timing is required.

Since rotation and magnification overlay depend on the location of pattern, the location shift caused by other type of overlay can affect the shift of rotation and magnification. However, the shifts are several nm which is relatively small compared with the location of pattern. To see the dependency of each overlay, we construct two types of random circuit consisted of ten logic depths. We use a different RC generation method for each case of circuit. One hundreds of circuits in each type are generated randomly.

TABLE I

Timing Errors ignoring the dependency.

	$Case1$	$Case2$
$Average(\%)$	0.007	0.011
$Std.Deviation(\%)$	0.020	0.036
$Avg.+3Std(\%)$	0.067	0.119

When we find θ to make the worst timing, ϕ and M are set to zero. θ and M are set to zero for finding ϕ of the worst case. Similarly, we find M when θ and M are zero. The exact variables to make the worst timing result are obtained by sweeping every variable in a given range. Since the number of variable to be swept is three, sweeping variables for entire search space is a time consuming procedure. In table I, we compare the timing result between the case of ignoring dependency and exact solution obtained by sweeping the variables. The difference is less than 0.119% in 3-σ level which is negligible. From this result, we see that one variable for the worst timing can be obtained by fixing other variables to zero.

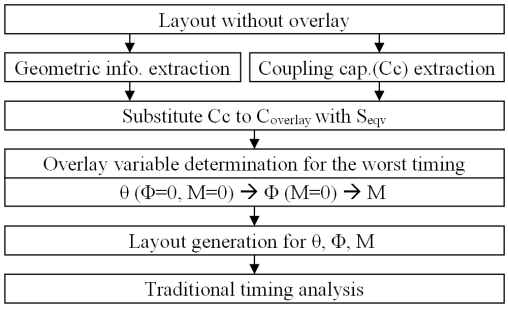


Fig. 13. Overlay aware timing analysis flow.

Figure 13 shows the timing analysis flow for a systematic overlay variation. Geometric information and coupling capacitance without overlay are extracted. Coupling capacitances are substituted to $C_{overlay}$. Since we do the variable searching consecutively, we can use the previously obtained variable as an initial point instead of zero. We could see that overlay variables obtained by the consecutive way is exactly the same with those obtained by sweeping simultaneously. The number of simulation to determine overlay variables for the worst timing is Nθ+Nϕ+NM where Nθ, Nϕ and NM is the number of simulation for sweeping θ, ϕ and M respectively. With the overlay variables, we can construct new metal layers considered the variation for the worst corner timing analysis. The best corner timing analysis can be done in a similar way.

V. Applications and results

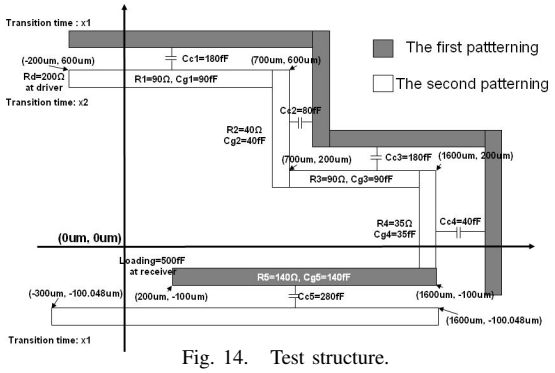


Fig. 14. Test structure.

In this section, we verify the accuracy of modeling and give an application example. Figure 14 shows a test structure used to verify the presented work. Our targeting interconnect for timing analysis is the one in the middle. Translation overlay will be dominated because the location of wire is close to the center. We assumed that α is 3nm, ϕ is $\pm$ 0.05 μ radian, M is $\pm$ 0.05ppm, and metal spacing without overlay is 48nm. This assumption is reasonable at 3-σ level [2]. We calculated the

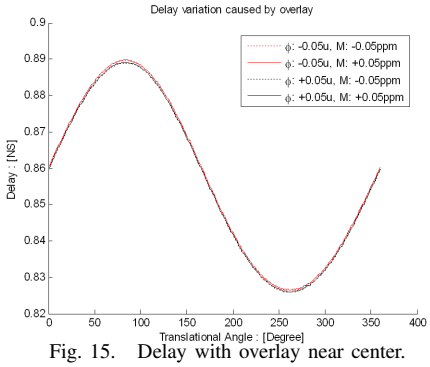


Fig. 15. Delay with overlay near center.

delay along the translation angle as shown in Figure 15. As we expected, rotation and magnification overlay is negligible because the position of interconnect is close to the center. The variation due to translation overlay is up to 7.8%.

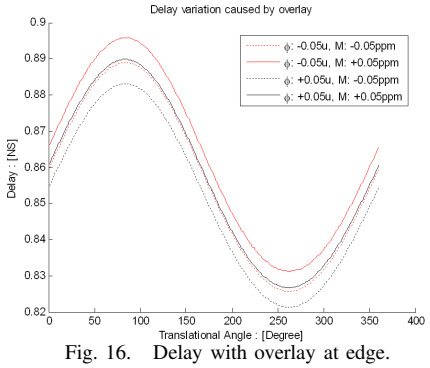


Fig. 16. Delay with overlay at edge.

To see the rotation and magnification overlay effect, the same layout in Figure 14 was shifted by (5000um,5000um). With the same overlay condition, the overall timing variation is 9.1%. The additional 1.3% variation comes from rotation and magnification overlay. When ϕ is negative, the delay increases because the counterclockwise rotation of the second patterning reduces spacing between metal layers. Similarly, if M is positive, the second patterning moves toward the first patterning. Thus, we can see the worst delay when M is positive value. With overlay vs. delay graph, we can see the variation effects for both the overall overlay and separated overlay source.

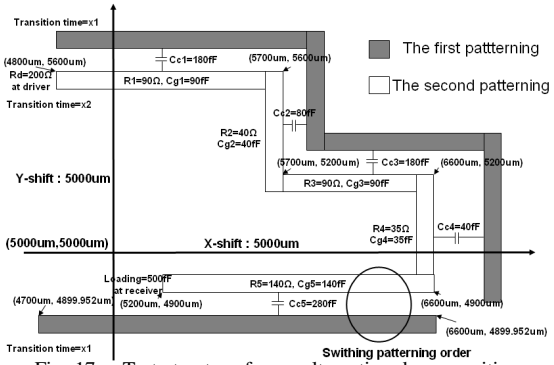


Fig. 17. Test structure for an alternative decomposition.

It is possible to optimize interconnect with overlay vs. delay graph. Figure 17 shows an alternative decomposition method for DPT which switches the patterning order of the lower part of targeting interconnect.

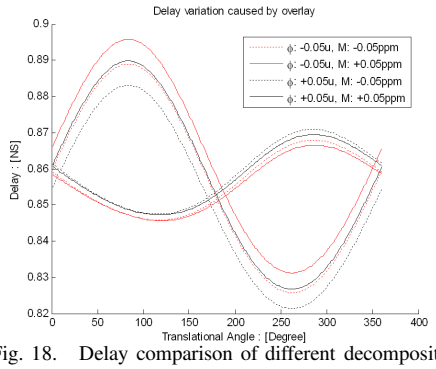


Fig. 18. Delay comparison of different decomposition.

The delay of two decomposition cases are compared in Figure 18. The decomposition in Figure 17 is more robust than the first one. The delay of the worst overlay case is 0.87ns which is 3% less than the first case. In the second decomposition, the variation range is 2.7% while the first decomposition case has 9.1% variation range. If there are two or more ways to decompose metal layer, we need a way to decide which one is better. Overlay vs. delay graph gives us a way to determine the optimized decomposition.

VI. CONCLUSIONS

We proposed a method to estimate the layout distortion due to overlay which is inevitable for DPT. We define several overlay variables such as the amplitude of translation overlay, the angle of rotation overlay, and the magnification factor. With a given overlay variable, we could model the parameterized coupling capacitance. We showed how to determine the overlay variables for the worst timing of a chip. In addition, we showed that different pattern decompositions vary in overlay tolerance. This work provides a way of designing a robust circuit with consideration of overlay.

REFERENCES

[1] Alfred K. Wong. *Resolution Enhancement Techniques in Optical Lithography*. SPIE Publications, 2001.

[2] W.-K. Ma, J.-H. Kang, C.-M. Lim, H.-S. Kim, S.-C. Moon, S. Lalbahadoersing, and S.-C Oh. Alignment system and process optimization for improvement of double patterning overlay. In *Proc. SPIE 6922*, 2008.

[3] D. Laidler, P. Leray, K. D'have, and S. Cheng. Sources of Overlay Error in Double Patterning Integration Schemes. In *Proc. SPIE 6922*, 2008.

[4] T.-B. Chiou, R. Socha, H. Chen, L. Chen, S. Hsu, P. Nikolsky, A. van Oosten, and A. C. Chen. Development of layout split algorithms and printability evaluation for double patterning technology. In *Proc. SPIE 6924*, 2008.

[5] N. Toyama, T. Adachi, Y. Inazuki, T. Sutou, Y. Morikawa, H. Mohri, and N. Hayashi. Pattern decomposition for double patterning from photomask viewpoint. In *Proc. SPIE 6521*, 2007.

[6] J.-S. Yang and A. Neureuther. Crosstalk Noise Variation Assessment and Analysis for the Worst Process Corner . In *Proc. Int. Symp. on Quality Electronic Design*, March 2008.

[7] P. Chen, D. A. Kirkpatrick, and K. Keutzer. Miller Factor for Gate-Level Coupling Delay Calculation. In *Proc. Int. Conf. on Computer Aided Design*, Nov 2000.

[8] A. B. Kahng, S. Muddu, and E. Sarto. On Switch Factor Based Analysis of Coupled RC Interconnects. In *Proc. Design Automation Conf.*, June 2000.

[9] Harry J. Levinson. *Principles of Lithography, 2nd Edition*. SPIE Publications, 2005.