Lithography-Aware Physical Design

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***Abstract*— Nanometer VLSI design is greatly challenged by the lithography limitations. Existing approaches in design for manufacturability (DFM) are mostly done *post* design, such as mask data preparation using various resolution enhancement techniques (RETs), rather than *during* design. To really bridge the gap between design and manufacturing, it is important to model and feed proper lithography metrics upstream to guide the proactive lithography aware physical design (LAPD). In this paper, we will discuss some key aspects of LAPD.**

I. Introduction

As VLSI technology continues to scale down to nanometer dimensions, the semiconductor industry is greatly challenged not only by many entangled *deep sub-micron* physical effects to reach *design closure* for timing, signal integrity, low power, etc., but also by *deep sub-wavelength* lithography limitations to reach the *manufacturing closure*, i.e., being manufactured reliably with high yield and robustness.

Among various manufacturing issues, lithography is probably the most fundamental one. Leading edge IC manufacturers still use 193nm lithography to print 90nm or smaller feature size, relying heavily on various and even exotic resolution enhancement techniques (RETs) [1], [2], such as optical proximity correction (OPC), phase shift mask (PSM) and off axis illumination (OAI) to modify the chip mask database (GDSII) and achieve better printability, higher yield, and less variability. However, these RETs are mostly done during post-tapeout mask synthesis at fabs, which may be too late to make all the necessary corrections or close silicon-based timing [3]. Meanwhile, RETs are not cheap (e.g., data volume increase by up to 10x, more mask write and inspection time). For a typical 90nm IC design process, 12 out of roughly 30 masks would require some form of resolution enhancement [2]. RET dramatically increases the mask cost, which has soared and reached $2 million per set at 90nm node. The semiconductor industry is adopting the immersion lithography, which will further extend the 193nm lithography to 45nm node or even below. Therefore, RETs will become more pervasive for future technology generations.

As the physical layout design and manufacturing closely relate to each other for nanometer VLSI, there is clearly a growing level of interdependency between them. A *true* design for manufacturability (DFM) flow is needed to *abstract* and *predict* the downstream manufacturing effects upstream into the key layout optimization stages, such as routing and placement, to preserve the true design intent, maximize the overall manufacturability, and minimize the overall manufacturing cost.

II. Lithography Aware Physical Design

In this section, we will first use routing as an example to consider the downstream lithography effects, then point out several key research aspects for lithography aware physical design.

To consider lithography effects during routing, one solution is to provide more and more routing rules by fabs to design houses and CAD tools. However, as technology moves to 90nm and beyond, the number of rules quickly explodes [4], [5], [6], [7]. This will significantly affect the router performance. In addition, there may be exotic rules hard for routers to resolve. Since the rule-based models usually lack accuracy, very conservative or restricted rules may have to be given [8]. Since these restricted design rules will be applied globally, the physical layout may be overly pessimistic. On the other hand, lithography simulations, though more accurate, could be very CPU intensive. It could easily take hundreds of CPU hours to run a full chip simulation-based OPC. Our experience with PROLITH [9] and SIGMA-C [10], two leading industry lithography simulation tools, shows that it could take a few minutes to simulate a 5um x 5um area (in accurate mode).

Thus it is desirable to directly link *fast* yet *high-fidelity* lithography simulations with the physical design such as routing and placement. There are very few works on this topic so far. The work by [11] is the first attempt to our best knowledge, where the optical interferences from neighboring edges are accumulated for an entire net under consideration. The interference, however, is not a direct measurement for the printability (as some interference may be "good" such as SRAFs).

In [12], a fast lithography simulator is developed which directly computes the edge placement error (EPE), which is essentially the critical dimension (CD) error at one side. The key idea of [12] is to decompose any partial coherent optical system into a small number of fully coherent systems, and use efficient table-look-up techniques. Our experience shows that reasonable fidelity with very fast simulation speed can be obtained, which can then be directly used to guide layout optimizations. Based on the fast lithography simulations, the concept of lithography hotspot map (LHM) is introduced for post-routing fixing on the difficult regions [12] (similar to congestion or thermal hotspots), for example those with large edge placement errors. Fig. 1 shows an example of EPE, which is the edge difference between the mask and the wafer. Since EPE is often used by RET tools to guide the mask synthesis [13], less EPE usually corresponds to less RET effort. The

EPE guided correction technique naturally fits into existing design flows and is capable of handling *full-chip* capacity. When the EPE map is generated, a ranked list of interfering neighboring edges can be stored. This information will be useful for RET-aware detailed routing with EPE guided wire spreading and rip-up and reroute [12]. An EPE guided post-routing optimization flow is shown in Fig. 2.

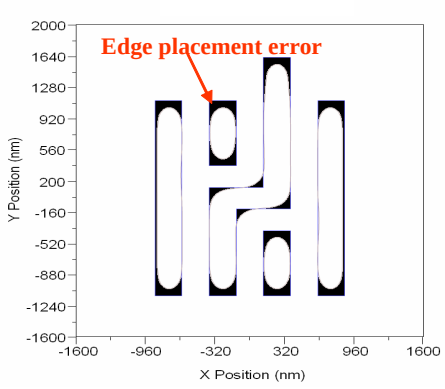

Fig. 1. Edge placement error map.

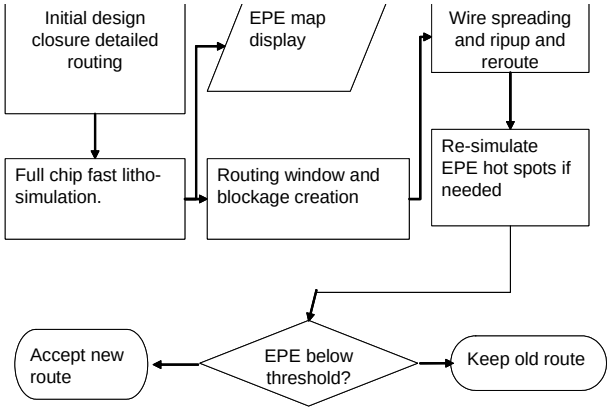

Fig. 2. EPE based detailed routing flow.

The algorithm in Fig. 2 is implemented in an industrial strength router and validated on some real 65nm industry designs. Fig. 3 shows the EPE hotspots (i.e., EPE bigger than certain threshold) before and after post routing optimization, such as wire spreading and rip-up and reroute. The number of EPE hotspots can be reduced by 40% after wire spreading and rip-up & reroute, by comparing Fig. 2 (a) and (c).

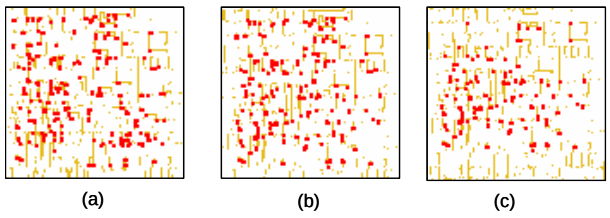

Fig. 3. (a) EPE map for the initial routing; (b) EPE map after the wire spreading; (c) EPE map after the rip-up & reroute.

It is encouraging to see such improvement with only post-layout optimization. It shall be noted that the work in [12] is just the first step toward the comprehensive lithography aware physical design (LAPD). By incorporating lithography effects early on, enabled by ultra-fast lithography models and metrics with high fidelity, many fundamental LAPD investigations can be done. For example, more accurate circuit optimizations can be performed so that the timing closure is not just achieved at the mask level, but at the "virtual" silicon image level. Litho-aware routing can be performed not just at the post-layout stage, but through the correct-by-construction routing using proper litho-cost to explore the design/manufacturing tradeoff. Furthermore, litho-aware placement shall be done to make sure no forbidden pitches exist between adjacent cells [14]. The placement also affects the overall interconnection, thus should be considered together with litho-aware routing.

III. Conclusion

For nanometer designs, it is important to model and predict the downstream lithography effects (such as printability and parametric yield) upstream into the key physical design stage to optimize the overall manufacturability and yield. We believe many research opportunities exist in such lithography aware physical design.

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