Wire Sizing with Scattering Effect for Nanoscale Interconnection

Sean X. Shi and David Z. Pan
Department of Electrical and Computer Engineering
University of Texas at Austin
Austin, TX 78712, USA
Email: sean.shi@mail.utexas.edu, dpan@ece.utexasedu

***Abstract*—For nanoscale interconnection, the scattering effect will soon become prominent due to scaling. It will increase the effective resistivity and thus interconnection delay significantly. Existing works on scattering effect are mostly performed using very complicated physics-based models, while the scattering impact on nanoscale VLSI interconnect and optimization have not been studied. In this paper, we first present a simple, closed-form scattering effect resistivity model based on extensive empirical studies on measurement data. Then we apply the proposed scattering model to revisit several classic wire sizing/shaping problems. Our experimental results show that if the scattering effect is ignored or characterized inaccurately beyond 65nm, the resulting interconnect optimization might be way off from the real optimal solution, e.g., up to 70% underestimation of the delay, or 20x oversizing. We also obtain the new closed-form wiresizing functions with consideration of scattering effects.**

I INTRODUCTION

As the feature size continues to shrink, the lateral dimension of conductors will be approaching the mesoscopic regime in which the diameter of the wire is in the range of or smaller than the mean free path of the electrons (λ, about 40*nm* for copper at room temperature), and the electrical resistivity of metallic conductors is increased compared to the resistivity of bulky metal. The earliest work on this dates back to 1938, when an expression for the resistivity of metal thin films (1-dimensional) was derived by Fuchs [1]. Later on it was extended to 2-dimensional by the FS model [2] for thin/narrow wires. Basically, the FS model accounts for the *surface* scattering. Later on, the MS model [3] was developed to incorporate the *grain boundary* scattering, which also increases the wire resistivity. For both surface and grain boundary scattering effects, very complicated quantum mechanical effects can be applied to obtain the empirical parameters in FS or MS model [4, 5].

While MS and FS models have been tested with measurement data for polycrystalline nanowires [6-8], very few experimental results on copper (Cu) film or interconnect have been reported until recently, e.g., the size effect of copper thin film was studied in [9], and the resistivity of copper wires with widths under 50nm was reported in [10-13]. The key observation is that the resistivity of copper wires will increase significantly as the wires width decreases [9-14]. While exploratory structures such as carbon nanotubes are being studied as possible replacement of copper interconnect [15-17], at least by 22nm technology, it is not likely that copper will be replaced by carbon nanotube or other materials [15]. There are also efforts in manufacturing improvement to partially reduce the scattering effect of copper wires [18, 19], but even so the scattering effect can no longer be ignored as the technology continues to scale down.

A popular method to reduce the interconnection delay is wire sizing. In fact, there have been a lot of works on it, e.g., the wire sizing and shaping without fringing capacitance [20, 21], with fringing capacitance [22, 23], under transmission line model [24], or with single-width sizing (1-WS) or two-width sizing (2-WS) [28]. Wire sizing for multi terminal nets have also been extensively studied [25-27]. However, all these previous wire sizing algorithms are based on the constant resistivity model without considering the scattering effects.

In this paper, we systematically study the impact of scattering effect on copper interconnection and wire sizing/shaping. Our key contributions include:

- Since existing physics-based scattering models are too complicated for nanoscale interconnect optimization, we propose a simple yet high-fidelity width-dependent resistivitiy model based on the experimental data for copper wire [10], thin film [9], and from ITSR 2004 [14]. Our proposed model fits well compared to these data with the regression coefficient $R \geq 0.999$.
- Based on our simplified closed-form model, we revisit various wire sizing issues with consideration of the scattering effect. As wire width shrinks, wire sizing will be more effective and necessary to reduce the interconnection delay because of scattering effect. Our experimental results also show that if the scattering effect is ignored or characterized inaccurately, the resulting interconnect optimization might be totally off from the real optimal solution, e.g., up to 70% delay

underestimation, or 20x over sizing.

- We obtain the new closed-form wire sizing functions with consideration of scattering effects, for both discrete wire sizing (with one sizable width), and continuous wire sizing (with infinite number of widths). The differences compared to those without scattering effects are pointed out.

The rest of the paper is organized as follows. In section II, we present the preliminaries and parameters used for our study [14, 28]. Section III presents our scattering effect modeling for resistivity of nanoscale Cu interconnection, and shows the delay impact caused by the scattering effect. The new wire sizing formulae and results are presented in Sections IV & V, followed by the conclusion in Section VI.

II PRELIMINARIES

This section presents the preliminaries and key parameters used in this paper. The driver of the interconnection is modeled as an effective resistance R_d connected to an ideal voltage source and a sink as a load capacitance C_L. The Elmore delay model [29, 30] is used to compute the interconnect delay. The notations for the key interconnect and device parameters include:

$w_{\min}$, minimum wire width, nm;
c_a, unit area capacitance, fF/μm;
c_f, unit effective-fringing capacitance, fF/μm;
c_g, input capacitance of a minimum device, fF;
r_g, output resistance of a minimum device, kΩ;
ρ_0, resistivity of Cu, assume no scattering, μΩ-cm;
$\rho_{\max}$, Max Cu resistivity of the minimum width, μΩ-cm;
AR, aspect ratio;
$t = w_{\min} \cdot AR$, metal thickness;
$R_d = r_g / 100$, driver resistance;
$C_L = 100 \cdot c_g$, load capacitance.

The basic parameters used in this paper are shown in Table 1. Note that these parameters are used mainly to illustrate the impact of scattering effect. The values are extracted according to [10, 14, 28, 31]. If necessary, more complete and specific parameters can be used.

Table 1 Basic Parameters

Year	2004	2007	2010	2013	2016
$w_{\min}$	90	65	45	32	22
c_g	0.0625	0.0573	0.0375	0.0246	0.0161
r_g	24.09	22.75	24.82	27.07	29.53
c_a	0.056	0.056	0.056	0.056	0.056
c_f	0.04	0.04	0.04	0.04	0.04
ρ_0	2.2	2.2	2.2	2.2	2.2
$\rho_{\max}$	3.35	3.79	4.49	5.42	6.88
AR	1.7	1.8	1.8	1.9	2

III SCATTERING EFFECT MODELING & IMPACT ON INTERCONNECTION DELAY

In this section, an empirical closed-form scattering effect model for nanoscale copper interconnect is proposed and validated, then it impact on interconnect delay is shown

A Model of Scattering Effect

Equation (1) (at the bottom of this page) shows the size-dependent part of the scattering effect model for metal wires, where only the grain boundary scattering (MS model [3]) is considered [8]. Obviously, such model is too complicated to be used for interconnection delay calculation and wire sizing. A simplified analytical model will be desirable for VLSI physical design applications.

B Simplified Closed-Form Model of Scattering Effect

Based on our empirical study on both MS and FS models and curve fitting, we obtain the following simple closed-form width-dependent resistivity model with scattering effect.

$$\rho(w) = \rho_B + \frac{K_\rho}{w} \tag{2}$$

Fig. 1 shows that the simple resistivity model fits well with the measured experimental data [10]. We have also verified this model based on the measurement data from [9] and the complicated model used in ITRS 2004 [14].

In the rest of this paper, we use the fitting parameters ρ_B=2.202 μΩ·cm, and K_ρ=1.030×10^{-15} Ω·m^2 based on [10]. Note that ρ_B is is almost the same as ρ_0, as when the dimension of Cu wire is large enough, the scattering effect can be ignored.

$$\frac{\rho_0}{\rho} = \frac{3}{4\pi hw}\int_{-h/2}^{h/2} dy \int_{-w/2}^{w/2} dx \int_{-\pi+\arctan(w/h)}^{\arctan(-w/h)} d\varphi \int_0^{\pi} \sin(\theta)\cos^2(\theta)\left[1-(1-p)\frac{\exp\left(-\frac{w}{2\lambda\cos(\theta)\cos(\varphi)}\right)}{1-p\cdot\exp\left(-\frac{w}{2\lambda\cos(\theta)\cos(\varphi)}\right)}\right] d\theta \tag{1}$$

$$+\frac{3}{4\pi hw}\int_{-h/2}^{h/2} dy \int_{-w/2}^{w/2} dx \int_{\arctan(-w/h)}^{\arctan(w/h)} d\varphi \int_0^{\pi} \sin(\theta)\cos^2(\theta)\left[1-(1-p)\frac{\exp\left(-\frac{w}{2\lambda\cos(\theta)\cos(\varphi)}\right)}{1-p\cdot\exp\left(-\frac{w}{2\lambda\cos(\theta)\cos(\varphi)}\right)}\right] d\theta$$

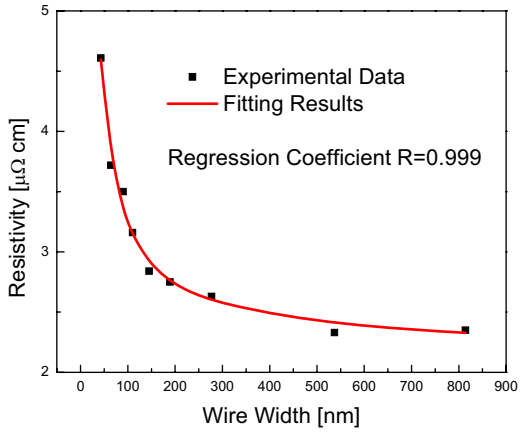

Fig.1 Resistivity of nanoscale wire. Observe that the resistivity *increases dramatically* as we decrease the wire width

C Impact of Scattering Effect on Interconnection Delay

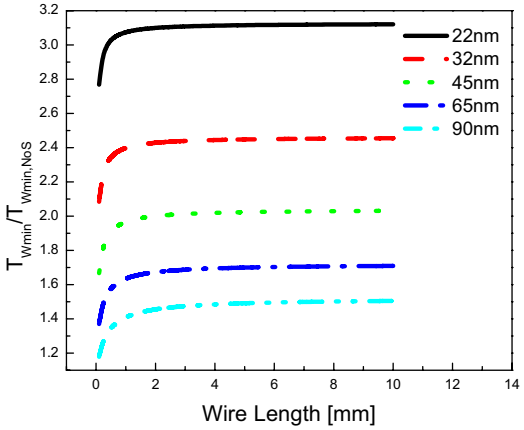

Fig.2 Normalized delay of different wirelengths under minimum wire width. The normalized delay is the ratio of delay with scattering effect to delay without scattering effect. Observe that the ratio is *always greater than 1* and it *worsens* with decreasing feature size.

The delay of single width wire including scattering effect can be written as follows

$$T_{1\text{-}WS} = R_d \cdot \left[c_a \cdot l \cdot w + c_f \cdot l + C_L \right] + \left[\frac{c_a \cdot l \cdot w}{2} + \frac{c_f \cdot l}{2} + C_L \right] \cdot \left[\rho_B + \frac{K_\rho}{w} \right] \cdot \frac{l}{w \cdot t} \quad (3)$$

where l is the wire length. In Fig. 2, the delay of the minimum width wires is calculated, and the ratio shows the delay with scattering effect over that without scattering consideration. We can see that in nanoscale manufacturing, scattering effect should be considered. Otherwise, interconnect delay may be underestimated significantly, and cause timing error.

IV Wire Sizing for Interconnect Delay and Area Estimation Based on Scattering Effect

In this section, we will derive the new wire sizing formulae based on the new width-dependent resistivity model with scattering effect Eqn.(1). Our experimental results show that scattering effect will have major impact on wire sizing in nanoscale interconnections.

A Efficiency of Wire Sizing

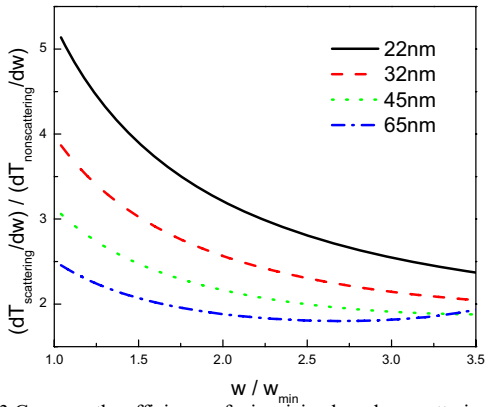

Fig.3 Compare the efficiency of wire sizing based on scattering and non-scattering. The efficiency defined as differential of delay over width. Wire length is 0.01 mm. Because of *scattering effect*, wire sizing beomes more effecient to reduce interconnection delay.

As mentioned in section III, in the nanoscale interconnection, scattering effect induces bigger resistivity, which in turn causes bigger delay. Thus, wider wires become more effective than before to compensate the more rapidly increase of wire resistance of narrow wires (additional effect due to increasing resistivity). In other words, wire sizing considering scattering effect becomes more efficient and more necessary. The efficiency of wire sizing can be defined as $\partial T/\partial w$, the sensitivity of delay reduction due to wire sizing. Eqn. (4) is the traditional wire sizing efficiency with a constant resistivity (bigger value can be used to mimic the impact of scattering effect). And (5) is the wire sizing efficiency with consideration of width-dependent scattering effect.

$$\frac{\partial T_{NonScattering}(w,l,S)}{\partial w} = R_d \cdot c_a \cdot l - \frac{1}{w^2} \cdot \left[\frac{1}{2} \cdot c_f \cdot \rho \cdot \frac{l^2}{t} + C_L \cdot \rho \cdot \frac{l}{t} \right] \quad (4)$$

$$\frac{\partial T(w,l,S)}{\partial w} = R_d \cdot c_a \cdot l - \frac{1}{w^2} \cdot \left[\frac{1}{2} \cdot c_f \cdot \rho_B \cdot \frac{l^2}{t} + C_L \cdot \rho_B \cdot \frac{l}{t} \right] - \frac{1}{w^2} \cdot \frac{1}{2} \cdot c_a \cdot K_\rho \cdot \frac{l^2}{t} - \frac{1}{w^3} \cdot \left[c_f \cdot \frac{l^2}{t} + 2 \cdot C_L \cdot \frac{l}{t} \right] \cdot K_\rho \quad (5)$$

In Fig. 3, wire sizing efficiencies with considering scattering and non-scattering are compared. It shows that wire sizing became more efficient than before where no scattering effect needs to be considered.

B 1-WS Model

In previous wire sizing and planning works [28], resistivity is assumed to be constant, and the optimal single width sizing (1-WS) can be calculated by:

$$w_{optimal,no-scattering} = \sqrt{\frac{c_f \cdot l + 2 \cdot C_L}{2 \cdot R_d \cdot c_a \cdot t}} \cdot \rho \qquad (6)$$

In nanoscale interconnection, the scattering effect is prominent. To calculated nanoscale interconnection delay, the resistivity of bulky Cu should be replaced by a bigger value to avoid underestimation of delay (see section III-C). But if we put (6) into the use of wire sizing of nanoscale interconnection just by replacing old resistivity with a bigger value (such as ρ_{max}, which is the resistivity of the minimum width wire of some specific technology node) and regarding this value as a constant, the optimal width of nanoscale Cu wire will be overestimated for the same reason that the resistance will decrease faster during wire width widening because of scattering effect.

According to (3), to minimize the interconnection delay, $\partial T_{1-WS}/\partial w = 0$. It becomes a cubic equation of wire width. Calculation shows that, from 130nm to 18 nm technology, only one real solution is bigger than the minimum wire width. The analytical function is shown as below:

$$w_{Optimal} = w_1 = 2\sqrt{\frac{a_1}{3}}\cos\left(\frac{\vartheta}{3}\right) \geq w_{\min} \qquad (7)$$

$$\text{where, } \vartheta = \cos^{-1}\left(\frac{K_\rho\left(c_f l + 2C_L\right)\sqrt{54 R_d c_a t}}{\left(c_a K_\rho l + c_f \rho_B l + 2C_L \rho_B\right)^{3/2}}\right)$$

$$a_1 = \frac{c_a K_\rho l + c_f \rho_B l + 2C_L \rho_B}{2 \cdot R_d \cdot c_a \cdot t}$$

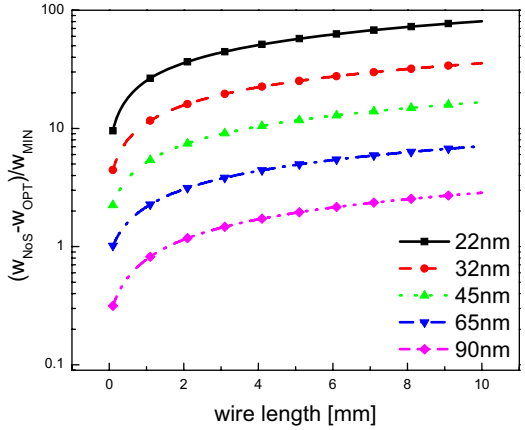

Fig.4 Compare of optimal wire sizing. The width diffrence is normalized in the way of being divided by minimum width. Observe that it is *alway bigger than 1* after 65nm node and it *worsens to more than 10x* after 22nm node.

Fig.4 compares the optimal wire sizes calculated without and with the width-dependent scattering effect (3). The optimal width of 1-WS with the constant resistivity ρ_{max} can be over 10 or 20x bigger than that of 1-WS with the width-dependent resistivity from scattering effect. This would cause excessive area waste and routability problem. On the other hand, if we use a smaller constant resistivity ρ_0 (in Table 1) for 1-WS, the resulting "optimal" width will be less, but such "optimal" delay can be much off from the real optimal obtained based on the width-dependent resistivity caused by the scattering effect. Using (7), the optimal wire width can be calculated, and the result of wire sizing is shown in Fig. 5. The delay can be reduced by 50-90% when using 1-WS optimization, compared to the minimum width.

Thus, it is very important to consider accurate scattering effect during the interconnect delay optimization and interconnect planning.

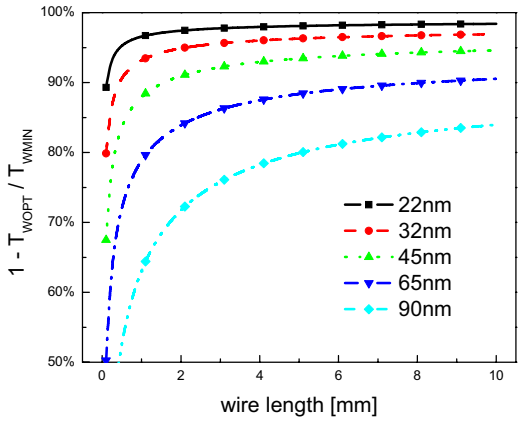

Fig.5 Delay reduction by wire sizing in nanoscale.

Because of *scattering effect*, interconnection delay can be efficiently reduced by wire sizing (compared with the delay of minum width wire).

V CONTINUOUS WIRE SIZING

In this section, continuous wire sizing/shaping is discussed. Different from classic wire shaping function [22], with the consideration of scattering effect, not only the theoretical solution but also the approximate solution will be more complicated than before.

A Euler's Differential Equation (math background)

$$I = \int_{x_0}^{x_1} F\left(x, u(x), u'(x)\right) dx$$

If *u(x)* is a function which can produce minimum *I*, according to [32], *u(x)* should satisfy Euler's Differential Equation:

$$F_u\left(x, u(x), u'(x)\right) = \frac{d}{dx} F_{u'}\left(x, u(x), u'(x)\right) \qquad (8)$$

B Wire Shaping to Minimize Elmore Delay

The wire shape can be defined as *f(x)*, and we define the terminal to contact driver R_d as $x=0$, the terminal to contact load C_L is $x=L$ (L is the wire length). As the scattering effect is considered, the function definition for Euler's equation is different from the previous work [22].

$$T = \int_0^L R_d \cdot \left[c_a \cdot dx \cdot f(x) + c_f \cdot dx + C_L \right] + \int_0^L \left[C_L + \int_0^x \left(c_a f(l) + c_f \right) dl \right] \left[\frac{\rho_B}{f(x)} + \frac{K_\rho}{f^2(x)} \right] \frac{dx}{t} = R_d \cdot C_L + \int_0^L F(x, u, u') \cdot dx \quad (9)$$

Where, $u(x) = \int_0^x f(l) \cdot dl$, $u'(x) = f(x)$

To minimize (9), Euler's equation (8) can be rewritten as

$$c_a (u')^2 \left[2\rho_B u' + 3K_\rho \right] + c_f u' \left[\rho_B u' + 2K_\rho \right] = \left[C_L + c_a u + c_f x \right] \left[2\rho_B \cdot u' + 6K_\rho \right] u'' \quad (10)$$

If

$$u(x) = \sum_{n=0}^{\infty} a_n \cdot x^n \quad (11)$$

For $a_0 = 0$ and a_1 is wire width at *x=0*. According to (10), $a_2, a_3, \cdots$ can be calculated one by one, for example, a_2 is:

$$a_2 = \frac{c_a a_1^2 \left(2\rho_B a_1 + 3K_\rho \right) + c_f a_1 \left(\rho_B a_1 + 2K_\rho \right)}{4C_L \left(\rho_B a_1 + 3K_\rho \right)}$$

C *Approximate Model*

The continuous wire sizing/shaping function f(x) can be approximated by $g_n(x)$ with different orders of accuracy.

$$g_1(x) = a_1; \quad g_2(x) = a_1 + \left(a_2 x + a_3 x^2 \right) / 2; \quad \cdots$$

$$g_n(x) = \sum_{i=1}^{2n-3} a_i x^{i-1} + \frac{1}{2} \left(a_{2i-2} x^{2i-3} + a_{2i-1} x^{2i-2} \right)$$

Fig. 6 shows the difference from $g_1(x)$ to $g_5(x)$ of 45nm technology. In most cases, the approximation using $g_3(x)$ is good enough to get the optimal wire shaping.

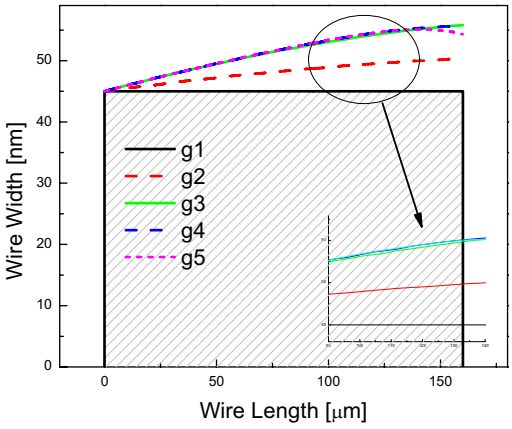

Fig. 6 Wire shaping with different order polynomial approximation

It shall be noted that $g_n(x)$ is different from [22], e.g., $g_3(x)$ is a quintic function while in [22] it is a cubic function. The scattering effect also increases the complexity of the approximate solutions.

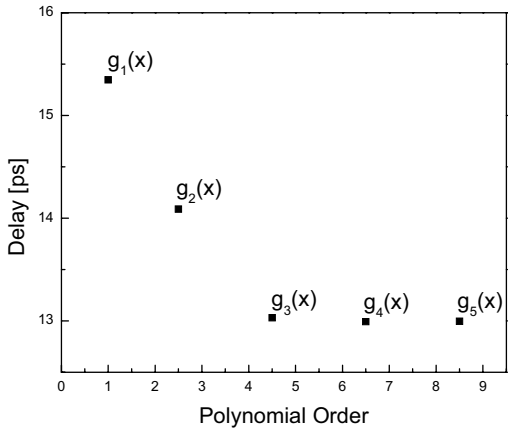

Fig. 7 Delay estimation of wire shaping (45nm node), compared of different orders of polynomial approximation. Observe that difference among g3, g4 and g5 is less than 0.5%

Fig.7 gives the delay comparison of different orders of polynomial approximation of wire shaping function. In this case, we can succeed reduce the interconnection delay by *18%* when using closed form $f(x)=g_3(x)$ of wire shaping instead of using minimum width $f(x)= g_3(x)=a_1$. From Fig.6, the area of wire just increase by *16%* for wire shaping. And closed form $f(x)= g_3(x)$ is accurate enough for wire shaping because the deference between this closed form function and more accurate ones are no more than 1%.

VI CONCLUSION

This paper studies an emerging topic for nanoscale interconnection, the scattering effect, as its impact on delay will soon become very important due to further technology scaling. We obtain a simple, width-dependent resistivity model due to scattering effect based on extensive empirical studies on measurement data. We then apply it to the classic wire sizing problems and show the importance of considering scattering effects for future interconnect optimizations.

To our best knowledge, this is the first work that addresses scattering effects on the nanoscale interconnect sizing. We plan to extend the model to consider other nanoscale effects such as the surface roughness.

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REFERENCES

[1] K. Fuchs, "The conductivity of thin metallic films according to the electron theory of metals," *Proc. Cambridge Philosophical Society*, 1938, pp. 100-108.

[2] E. H. Sondheimer, "The Mean Free Path of Electrons in Metals," *Adv. Phys.*, vol. 1, pp. 1-42, 1952.

[3] A. F. Mayadas and M. Shatzkes, "Electrical-Resistivity Model for Polycrystalline Films: the Case of Arbitrary Reflection at External Surfaces," *Phys. Rev*, vol. B 1, pp. 1382–1389, 1970.

[4] Z. Tesanovic, M. V. Jaric, and S. Maekawa, "Quantum Transport and Surface Scattering," *Phys. Rev. Lett.*, vol. 57, pp. 2760-2763, 1986.

[5] R. Dannenberg and A. H. King, "Behavior of grain boundary resistivity in metals predicted by a two-dimensional model," *Journal of Applied Physics*, vol. 88, pp. 2623, 2000.

[6] J. Vancea, "Unconventional Features of Free Electrons in Polycrystalline Metal Films," *International Journal of Modern Physics B*, vol. 3, pp. 1455-1501, 1989.

[7] J. Vancea, G. Reiss, and H. Hoffmann, "Mean-free-path concept in polycrystalline metals," *Phys. Rev. B*, vol. 35, pp. 6435-6437, 1987.

[8] C. Durkan and M. E. Welland, "Size effects in the electrical resistivity of polycrystalline nanowires," *Phys. Rev. B*, vol. 61, pp. 14215–14218, 2000.

[9] S. M. Rossnagel and T. S. Kuan, "Alteration of Cu conductivity in the size effect regime," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 22, pp. 240, 2004.

[10] W. Steinhoegl, G. Schindler, G. Steinlesberger, and M. Engelhardt, "Size-dependent resistivity of metallic wires in the mesoscopic range," *Physical Review B (Condensed Matter and Materials Physics)*, vol. 66, pp. 075414, 2002.

[11] G. Steinlesberger, M. Engelhardt, G. Schindler, W. Steinhogl, A. v. Glasow, K. Mosig, and E. Bertagnolli, "Electrical assessment of copper damascene interconnects down to sub-50 nm feature sizes," *Microelectron. Eng.*, vol. 64, pp. 409-416, 2002.

[12] W. Wen and K. Maex, "Studies on size effect of copper interconnect lines," *Proc. International Conference on Solid-State and Integrated-Circuit Technology (ICSICT)*, 2001, pp. 416.

[13] C.-U. Kim, J. Park, N. Michael, P. Gillespie, and R. Augur, "Study of Electron-Scattering Mechanism in Nanoscale Cu Interconnects," *Journal of Electronic Materials*, vol. 32, pp. 982-987(6), 2003.

[14] "International Technology Roadmap for Semiconductors (ITRS)," 2004.

[15] A. Naeemi, R. Sarvari, and J. D. Meindl, "Performance comparison between carbon nanotube and copper interconnects for gigascale integration (GSI)," *Electron Device Letters*, vol. 26, pp. 84, 2005.

[16] A. Raychowdhury and K. Roy, "A circuit model for carbon nanotube interconnects: comparative study with Cu interconnects for scaled technologies," *Proc. ICCAD*, 2004, pp. 237.

[17] N. Srivastava and K. Banerjee, "A Comparative Scaling Analysis of Metallic and Carbon Nanotube Interconnections for Nanometer Scale VLSI Technologies," *Proc. the 21st International VLSI Multilevel Interconnect Conference (VMIC)*, Waikoloa, HI, 2004, pp. 393-398.

[18] P. Kapur, J. P. McVittie, and K. C. Saraswat, "Technology and reliability constrained future copper interconnects. I. Resistance modeling," *TED*, vol. 49, pp. 590, 2002.

[19] S. H. Brongersma, K. Vanstreels, W. Wu, W. Zhang, D. Ernur, J. D'Haen, V. Terzieva, M. Van Hove, T. Clarysse, L. Carbonell, W. Vandervorst, W. De Ceuninck, and K. Maex, "Copper grain growth in reduced dimensions," *Proc. Interconnect Technology Conference*, 2004, pp. 48-50.

[20] J. P. Fishburn and C. A. Schevon, "Shaping a distributed-RC line to minimize Elmore delay," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 42, pp. 1020, 1995.

[21] C.-P. Chen, Y.-P. Chen, and D. F. Wong, "Optimal wire-sizing formula under the Elmore delay model," *Proc. DAC*, 1996, pp. 487.

[22] J. P. Fishburn, "Shaping a VLSI wire to minimize Elmore delay," *Proc. European Design and Test Conference*, 1997, pp. 244 - 251.

[23] C.-P. Chen and D. F. Wong, "Optimal Wire-sizing Function With Fringing Capacitance Consideration," *Proc. DAC*, 1997, pp. 604.

[24] Y. Gao and D. F. Wong, "Shaping a VLSI wire to minimize delay using transmission line model," *Proc. ICCAD*, 1998, pp. 611.

[25] J. J. Cong and K.-S. Leung, "Optimal wiresizing under Elmore delay model," *TCAD*, vol. 14, pp. 321, 1995.

[26] C. C. N. Chu and D. F. Wong, "An efficient and optimal algorithm for simultaneous buffer and wire sizing," *TCAD*, vol. 18, pp. 1297, 1999.

[27] J. Cong and Z. Pan, "Interconnect performance estimation models for design planning," *TCAD*, vol. 20, pp. 739, 2001.

[28] J. Cong and Z. Pan, "Wire width planning for interconnect performance optimization," *TCAD*, vol. 21, pp. 319, 2002.

[29] W. C. Elmore, "The Transient Response of Damped Linear Networks with Particular Regard to Wideband Amplifiers," *Journal of Applied Physics*, vol. 19, pp. 55, 1948.

[30] J. Rubinstein, P. Penfield, and M. A. Horowitz, "Signal Delay in RC Tree Networks," *TCAD*, vol. 2, pp. 202, 1983.

[31] S. Borkar, "Design challenges of technology scaling," *Micro*, vol. 19, pp. 23, 1999.

[32] L. Euler, *Methodus inveniendi lineas curvas maximi minimive proprietate gaudentes sive solutio pro blematis isoperimetrici lattissimo sensu accepti*. Lausanne, Geneva, 1744.