A Unified Non-Rectangular Device and Circuit Simulation Model for Timing and Power

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***Abstract*— For 65nm and below devices, even after optical proximity correction (OPC), the gate may still be non-rectangular. There are several limited works on the device and circuit characterizations for the post-OPC non-ideal-shape wafer images, with significant impacts on timing and power. Most of them, however, are based on the equivalent gate length models, which are different for timing and leakage, and thus hard to use for coherent circuit simulations. In this paper, we propose a unified post-litho device characterization model and circuit simulation for timing and power. To our best knowledge, this is the most accurate methodology for post-litho analysis, including timing, leakage and transient simulation. Based on this method, the parameter extraction is also included in the model which was omitted by previous works. A post-litho model card is proposed for circuit simulation to combine these two techniques. Our experimental results validate the new model.**

I. Introduction

As the IC technology evolves toward nanometer scale dimensions with higher densities, the printability of fine lithographic patterns with rectangular shapes is rapidly reduced due to the fundamental limit of both microlithography systems and process variations. As 193nm lithographic system is still used to print critical dimension (CD) of 65nm (and likely 45nm or even below feature size), various resolution enhancement techniques (RET), including optical proximity correction (OPC), phase shift mask (PSM), off-axis illumination (OAI) are used to push the lithographic systems to their limits.[1] Even with extensive RETs, the gate shapes may still be away from perfect rectangles which impact the timing of the whole chip [2]. Meanwhile, different process variations, such as dose, focus, etching variations, can push the manufactured silicon image (SI) of the gate even further away from the design-intended rectangle layout. In fact, as the channel region is determined by the interfaces between dopant profiles of channel and source/drain under the poly gate, the recent paper [3] has shown that even under rectangular gate, the channel region may be seriously still non-rectangular, which makes the rectangular gate effectively non-rectangular. As the continuous shrinkage of feature sizes, non-rectangular gates and channels are unavoidable due to the limitation of manufacturing process and have to be dealt with and simulated accurately.

The non-rectangular property of the gate SI has received a lot of research attention recently. It was first treated as random variations on the edges of the gate, i.e., line edge roughness (LER) [3-7]. The devices with LER can be simulated by 3D TCAD methods but they are too slow to be performed for circuit level simulation and optimization. A commonly used technique is gate slicing which applies 2D TCAD to study LER [5, 7]. As the non-rectangular of channel shape is most directly decided by the gate shape, the non-rectangular gate can be directly used to predict the channel shape. Recent works [8-10] use gate slicing and *equivalent gate length* (EGL) methods to simulate the impact of non-rectangular gate shapes in SPICE which is much faster than TCAD software. Two EGLs of each device are defined to replace the original uniform gate length set on layout: ON EGL for timing issues when the device is turned on and OFF EGL for leakage issues when the device is cutoff.

Although EGLs can model a non-rectangular device in either of its two specific working states (ON/OFF) well, they are hard to be used for coherent circuit simulations in practice, since it is often difficult to tell when and which devices are absolutely on or off for complicated cell schematics, thus it is hard to choose the right EGL for circuit simulation. Another limitation of these EGL works [8-10] is that they only studied the performance difference between non-rectangular and ideal rectangular gates. In fact, device models, such as BSIM3, BSIM4 [11], and PTM [12], and their parameters are extracted from the real devices with certain non-rectangular shapes. So the impact of gate shape with certain non-rectangles on device performance has been already included in the device models [10]. Performance simulations of gates between different non-rectangular shapes are necessary and crucial, or the impact of non-rectangular gate shape may be overestimated.

In this paper, we propose a novel unified non-rectangular device and circuit simulation model/methodology. Different from previous works of revalue specific parameter such as gate length, our work modifies the whole range of drain-source current model which is much more accurate than the two EGLs of ON and OFF. Meanwhile, the impact of nonrectangular gate shape during parameter extraction of device model (BSIM or PTM) can be fully considered. Moreover, as an additional device modeling card, it is based on I-V properties of the devices, and thus it can be integrated to any existing device models for post-lithography device/circuit simulation.

The rest of this paper is organized as follows: in section II, general model extraction flow including gate slicing is reviewed, with other preliminaries for our unified post-litho non-rectangular model. The details of post-litho device modeling card are discussed in Section III. Section IV shows how to integrate the modeling card into design flow and how to implement circuit

simulation with the consideration of lithographic process variations. Simulation results are shown in Section V with the comparison between EGL and our unified model, as well as the impact of lithographic variations. An interesting observation is that in some cases, lithographic variations of defocus may be helpful in both timing and power. Conclusion is in the last section VI.

II. Preliminary

In this section, the gate slicing method is presented. With the consideration of narrow width effect during gate slicing and current calculation, a new drain-source current can be calculated according to the current combination formula (1). Previous EGL methods are extracted from the new current under some specific working states as shown in part D.

A. Gate Slicing

The practical gates are never rectangles of a uniform channel length or width. As the channel width is much bigger than channel length in nanometer designs, the relative variations of channel width are much smaller than that of channel length. As [9], the equivalent channel width is calculated according to the same gate shape area at the width edge of the channel.

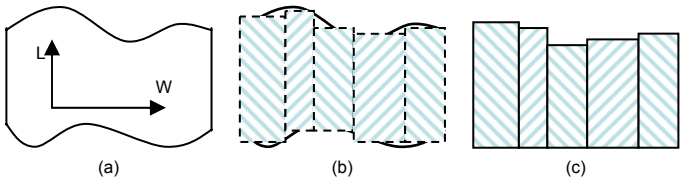

Fig.1 Slicing of a non-rectangle/non-uniform gate shape.

Previous LER papers [4, 7] have shown that slicing is a reliable method to simulate the channel length variations within a gate. And many post-OPC EGL papers [8-10] use this slicing method to study the impact of OPC.

After layout is designed and OPC is finished, the silicon image of each gate can be got as shown in Fig.1 (a). Set W_0 as the channel width. Then in the second step, the gate is sliced into small pieces along the channel width direction (Fig.1 (b)). Each slice of the gate represents a single device with different channel lengths as shown in Fig.1 (c).

B. Narrow Width Effect

If the width of slice i is ΔW_i, the length is L_i, the single device of slice i can be simulated by SPICE software. As the slicing process is just an artificial method, during the simulation, the device width of a single slice can not be regarded as a ΔW_i, or the narrow width effect will be seriously overestimated.

One way to eliminate the narrow width effect is to simulate two devices with width of ($W'+\Delta W_i$) and (W'), and use the current difference as the current of the sliced device [9], where W' is a large device width. The disadvantage of this method is that when ΔW_i is not small enough, the contribution of narrow width effect can not be as accurate as the original.

In this paper, a better way is used to accurately simulate the impact of narrow width effect by widening the width of a slicing device from ΔW_i back to its original size W_0. Then the drain-source current of each slice is $I_{ds,i}(L_i, W_0, V_{ds}, V_{gs})*\Delta W_i/ W_0$.

C. Current combination

After each of the slices is simulated according to its channel length, width, V_{gs}, V_{ds}, the drain-source current of the original gate with certain SI is calculated as formula (1).

$$I_{ds}\left(SI, V_{ds}, V_{gs}\right) = \sum_{i=1}^{n} I_{ds,i}\left(L_i, W_0, V_{ds}, V_{gs}\right) \cdot \Delta W_i / W_0 \qquad (1)$$

where $$\sum_{i=1}^{n} \Delta W_i / W_0 = 1$$

D. Equivalent Gate Length for ON and OFF state

From formula (1), EGL can be defined as the gate length function of V_{gs} and V_{ds} to keep the gate have the same drain-source current under certain V_{gs} and V_{ds} as shown in below.

$$I_{ds}\left(L_{eq}\left(V_{ds}, V_{gs}\right), W_0, V_{ds}, V_{gs}\right) = I_{ds}\left(SI, V_{ds}, V_{gs}\right) \qquad (2)$$

In [8-10], EGL for ON and OFF state are used to calculate the impact of non-rectangular gate with uniform gate length. An NMOS is ON when $V_{gs}>V_{th}$, and OFF when $V_{gs}<V_{th}$. And if the impact of V_{ds} on the drain-source current is omitted, we can have the EGL of ON and OFF state separately.

$$I_{ds}\left(L_{eq,ON}, W_0\right) = I_{ds}\left(SI\right) \quad when \ \left(V_{gs} > V_{th}\right)$$
$$I_{ds}\left(L_{eq,OFF}, W_0\right) = I_{ds}\left(SI\right) \quad when \ \left(V_{gs} < V_{th}\right)$$

From this function, we can see the limitation of previous EGL works: the impact of different values of V_{ds} and V_{gs} is simplified and omitted and EGL method is just suitable some discrete cases from the continuous working states of a device. In the results section, impact of V_{ds} and V_{gs} on equivalent gate lengths is shown to be quite obvious. Moreover, in complicated cell schematics, it is difficult to tell when to use ON or OFF EGL, especially in an automatic way.

III. Post-Litho Device Modeling Card

In this section a new post-litho device modeling card is developed directly from the drain-source current formula (1) to model of non-rectangular gates after lithographic process simulation. Different from previous works [8-10] which use EGLs to replace original values of uniform gate lengths in SPICE simulation, our post-litho device modeling card can more precisely simulate the impact of length variations within a single gate by continuously modifying the source/drain current.

The comparison between gates of different non-rectangular shapes is considered in this model. The parameters of device models such as BSIM3, BSIM4 [11], and PTM [12] and their parameters are extracted from the experimental results of real devices after manufacturing, and the gate shapes/SIs of manufactured devices are never rectangular with a uniform channel length. Therefore the impact of some specific non-rectangular gate shape on the device electrical performance has already been involved in the huge number of parameters of device models. Previous EGL methods assume that those device models (BSIM or PTM) are extracted from perfect rectangular gate with constant channel lengths. This assumption is not reliable and will overestimate the impact of channel length variations within a gate. The post-litho modeling card presented

in this section is able to model the precise performance difference between devices of two non-rectangular SI, and non-rectangular SI information of the device models can be well considered in this modeling card.

Different from EGL methods, our device modeling card calculates the drain-source current difference of different SI devices. As it is extracted directly from the device I-V properties, it is independent on any device models and can be integrated with any existing device models. In our modeling card, to get the drain-source currents $I_{ds,i}(L_i, W_0, V_{ds}, V_{gs})$ in (1), we model it in part A, B, C based on current curve fitting functions and give the final device model in part D.

A. Current Modification Function of a Single Gate Slice

In formula (1), to calculate the I-V curves $I_{ds,i}(SI, V_{ds}, V_{gs})$ of any SI under certain gate-source and drain-source voltage, the current $I_{ds,i}(L_i, W_0, V_{ds}, V_{gs})$ of certain channel length L_i and width W_0 should be known. So, current $I_{ds,i}(L_i, W_0, V_{ds}, V_{gs})$ are precalculated and collected in our model, and function (3) are used to fit the data to reduce the database and speedup the simulation.

According to our I-L curve fitting experience, function (3) is adopted for its better fitting of the drain-source current-length curves at different V_{gs} and V_{ds} with different values of three fitting parameters a_2, b_2, and c_2. The disadvantage of this function is that these three parameters are not consistent when V_{gs} and V_{ds} change. So ΔI_{ds} is calculated and stored for the consistency purpose during interpolation.

$$I_{ds} = \exp\left(a_2 + b_2 \cdot L + c_2 \cdot L^2\right) \tag{3}$$

$$\begin{aligned} &\Delta I_{ds}\left(L, W, V_{gs}, V_{ds}\right) \\ &= \exp\left(a_2 + b_2 L + c_2 L^2\right) - \exp\left(a_2 + b_2 L_0 + c_2 L_0^2\right) \end{aligned} \tag{4}$$

where L_0 is design-intended gate length.

B. Post-Litho Device Modeling Card from Rectangular to Non-Rectangular Device Modeling

After collecting the drain-source current data of uniform device, silicon image of designed layout can be simulated by lithographic simulators. If we have the device model of perfect rectangular gate, the difference of the drain-source current between a non-rectangular gate of real SI and an ideal rectangular gate of uniform channel length can be calculated. The current difference of the same width and working state with different lengths, $[I_{ds,i}(L_i, W_0, V_{ds}, V_{gs}) - I_{ds}(L_0, W_0, V_{ds}, V_{gs})]$ in (5).

$$\begin{aligned} &\Delta I_{ds,real}\left(SI, V_{ds}, V_{gs}\right) \\ &= I_{ds}\left(SI, V_{ds}, V_{gs}\right) - I_{ds}\left(L_0, W_0, V_{ds}, V_{gs}\right) \\ &= \sum_{i=1}^{n}\left[I_{ds,i}\left(L_i, W_0, V_{ds}, V_{gs}\right) - I_{ds}\left(L_0, W_0, V_{ds}, V_{gs}\right)\right] \cdot \Delta W_i / W_0 \end{aligned} \tag{5}$$

C. Model Extraction for Rectangular Gate Device

1) Parameter Extraction of Device Modeling

As mentioned before, the parameter extraction of BSIM or other device modeling is based on the tests of practical manufactured devices and the impact of certain non-rectangle gate shapes on device performance has already been captured into the model [10]. However, a large number of parameters in those device models are needed to fit the difference between experimental data and theoretical models.

2) Non-Rectangle to Non-Rectangle Mapping

So the right post-OPC device characterization should transform device model of specific non-rectangular gates (such as BSIM with parameters supplied by fabs) to the device model of a different general non-rectangle gate, which varies due to different RET/OPC strategies, different layout environments, and different manufacturing process variations.

3) Device Model for Rectangular gate

Formula (6) gives the current difference between gate with SI_{EX} (the silicon image of the gate for device model parameter extraction) and a corresponding rectangle device. So the current of ideal rectangle device can be calculated by subtracting $\Delta I_{ds,EX}$ from current simulation results of SPICE based on BSIM or PTM model using formula (1), where $I_{ds}(L_0, W_0, V_{ds}, V_{gs})$ is the drain-source curve of perfect rectangular devices.

$$\begin{aligned} &\Delta I_{ds,EX}\left(SI_{EX}, V_{ds}, V_{gs}\right) \\ &= I_{ds}\left(SI_{EX}, V_{ds}, V_{gs}\right) - I_{ds}\left(L_0, W_0, V_{ds}, V_{gs}\right) \end{aligned} \tag{6}$$

D. Post-Litho Device Modeling Card

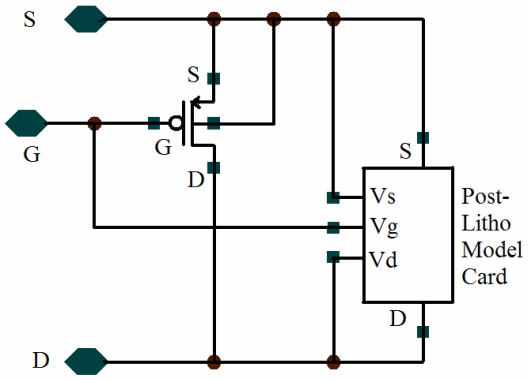

Fig.2 Module Schematic of post-litho device modeling card.

From (5) and (6), the drain-source current difference of post-litho device can be calculated as the post-litho modeling card as shown in (7). And it will be added to each MOSFET with any existing device model to modify the drain-source current by a value of $[\Delta I_{ds,real}(SI, V_{ds}, V_{gs}) - \Delta I_{ds,EX}(SI_{EX}, V_{ds}, V_{gs})]$ with the SI information as the input arguments. Each MOSFET will be replaced by a post-litho module made up of other original MOSFET with uniform gate length with an additional post-litho modeling card as shown in Fig.2.

$$\begin{aligned} &I_{ds,real\_EX}\left(SI, V_{ds}, V_{gs}\right) - I_{ds}\left(L_o, W_0, V_{ds}, V_{gs}\right) \\ &= \Delta I_{ds,real}\left(SI, V_{ds}, V_{gs}\right) - \Delta I_{ds,EX}\left(SI_{EX}, V_{ds}, V_{gs}\right) \end{aligned} \tag{7}$$

IV. Post-Litho Circuit Simulation Flow

In this section, the circuit/cell level simulation flow is proposed based on the post-litho device modeling card in the previous section. Instead of two values of equivalent gate lengths, the post-litho modeling card modified the I-V curve of a single device under certain SI with continuous working states (under different V_{gs} and V_{ds}), and thus much more cell level simulation can be performed based on the modeling card.

Fig.3 shows the post-litho circuit simulation flow of this work.

The *ΔI-L* of devices from (4) and (6) is precalculated and stored in the post-litho device modeling card. The SI information of each gate is input as the arguments to the modeling card, and each MOSFET in original circuit schematics is modified by the corresponding modeling card (as shown in Fig.2). Post-litho circuit simulation is performed based on the new schematics.

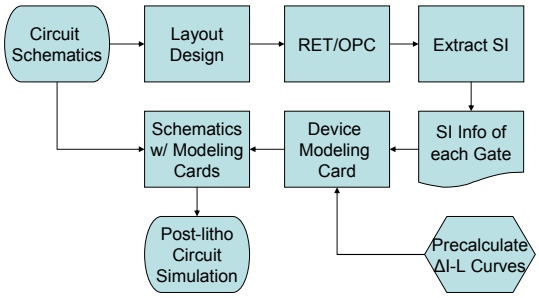

Fig.3 Post-litho circuit simulation flow

As the process variations will change the silicon image of devices, the impact of lithographic relative process variations (such as defocus and variations of dose [14]) on the circuit electrical performance can also be precisely simulated using the post-litho device modeling card.

V. Results

The simulation results are shown in this section. As the drain current of non-rectangular devices are various with different V_{gs} and V_{ds}, the uncertainty of EGL of different device working states are studied in part A. As mentioned in section II part D, the ON and OFF ELG are only accurate for some specific discrete working states, the post-litho device modeling card without considering SI_{EX} is verified under those working states in part B.

After considering the non-rectangular gate shapes for device model parameter extraction, timing issues (delay and slew) and power issues (dynamic and static) of an inverter are discussed in part C, D and E. In part C, compared to our post-litho modeling card, about 2% underestimation of delay and slew of ON EGL method is observed. The precise simulations also show that lithographic process variations (especially defocus) can induce 15% difference on timing, and impact rising and falling delays differently.

In part D our test case shows that neglecting the impact of SI_{EX}, the power estimation (dynamic and static) of EGL method can be seriously wrong (*10%* to *1.5X*). And certain lithographic defocus can greatly reduce dynamic power consumption while slightly increase the static power. In part E, the power supplied directly from voltage source V_{dd} is studied. Results show that EGL method can be seriously wrong (up to 30% for static power) and lithographic variations may greatly increase the power consuming/load supplied by V_{dd}, which can induce more challenge on power distribution.

A. Uncertainty of Equivalent Gate Length

As mentioned above, at different V_{gs} and V_{ds}, the post-litho drain-source current is different, and the EGL in (2) should vary. As a function of V_{gs} and V_{ds}, more accurate values of EGL are calculated according to (2). Fig.4 shows the ranges of EGLs of NMOS are various at different V_{gs}, and even for the same V_{gs}, different values of V_{ds} also induce different EGLs.

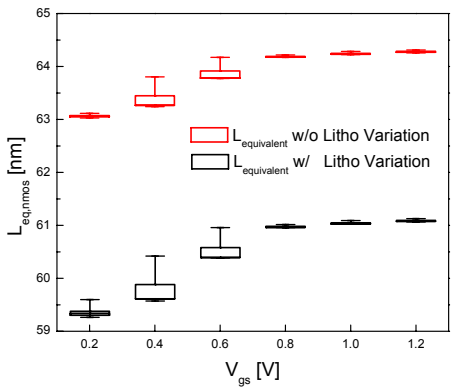

Fig.4 Different EGL of NMOS

Fig.5 shows the different variation ranges equivalent gate lengths of PMOS under different V_{gs} with various V_{ds}. Compared to NMOS, one interesting issue of PMOS in our test case is that under the same V_{gs}, the variations of the PMOS equivalent gate lengths are much bigger than that of NMOS and the equivalent lengths are much more strongly dependent on the V_{ds}.

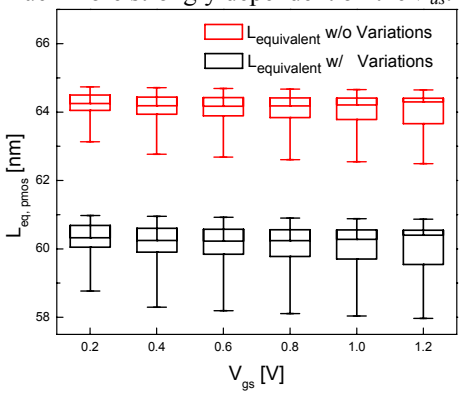

Fig. 5 Different EGL of PMOS

After considering the lithographic variations (defocus and dose variations), the EGL will be changed obviously. According to our simulation cases, the lithographic variations of defocus will induce the decrease of EGL.

From above results, EGLs of NMOS/PMOS varies in a big range under different V_{gs} and V_{ds}. 2 ON/OFF values of EGL are not enough for accurate simulation.

B. Verification of Post-Litho Device Modeling Card

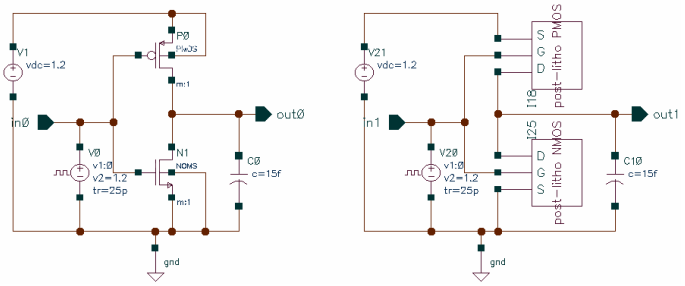

Fig.6 Schematic circuit for module verification

The post-litho device module (Fig.2) is verified in the circuit level simulation. In Fig.6, an inverter is simulated to compare voltage, current, timing and power issues of post-litho modeling

card with EGL methods. The input is a pulse voltage between 0V and 1.2V with 2ns period and 25ps rising and falling time. The load capacitance is 15fF. Note that to verify the module of modeling card under the same assumption, the modeling card in this section does not involve the impact of the non-rectangle gate shape/SI of device models which is not considered by EGL method.

Fig.7 is the leakage current through the drain when the state of the PMOS is in an absolutely OFF state. Comparing with EGL of ON state or uniform 65nm gate length, the drain current of post-litho model can *absolutely* overlap with the points of drain current of EGL of OFF state.

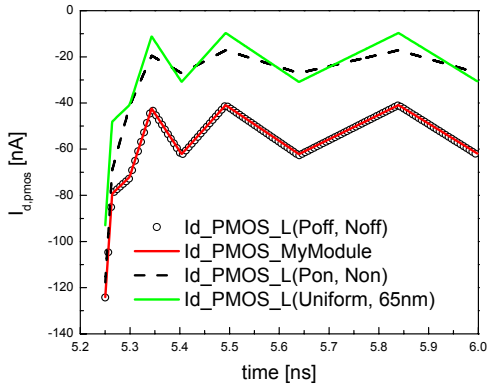

Fig.7 Leakage current through drain of PMOS

From Fig.8, the device modeling card module (red curves) are quite close to the V_{out} points simulated by ON equivalent gate length, especially at middle voltage value of 0.6V which is used to define the circuit delay. The delay data of different methods can be found in Table 1.

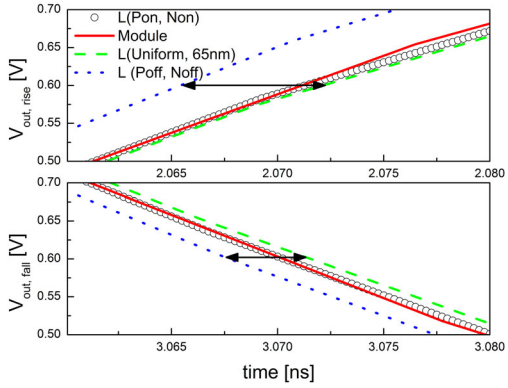

Fig.8 V_{out} curves for timing comparison

Table 1 gives output delay comparison between different method. "ON EGL" mean that the gate lengths of devices in the cell schematics are set to be their ON equivalent gate length, while "OFF EGL" means all devices use their OFF EGL. "L=65nm" is for the devices with the uniform 65nm gate length. "Our Model" means our post-litho unified non-rectangular device characterization and circuit simulation method.

Table 1 Output Delay Comparison

	Rising Delay		Falling Delay	
	(ps)	dif.	(ps)	dif.
ON EGL	58.8	-	57.8	-
L=65nm	59.6	1.42%	59.1	2.21%
OFF EGL	52.6	-10.5%	55.2	-4.43%
Our Model	58.6	**-0.28%**	57.8	**0.01%**

The simulation results of leakage and timing in this part validate our post-litho device modeling card (all errors are less than 0.5%) under extreme conditions when devices are fully ON and OFF.

C. *Timing Results of Post-Litho Circuit Simulations*

After verifying the unified device modeling card, complete modeling cards (with the consideration of non-rectangular SI_{EX}) are used for timing analysis of post-litho circuit simulation. The delay comparison is in Fig. 9 and Table 2, while slew part is in Table 3.

Fig. 9 shows the rising/falling delay of ON EGL method, our unified model without and with variations. Table 2 compares the delay by different simulation methods and conditions, while Table 3 is for slew. The light arrows in Fig.9 show the delay from V_{in} to V_{out}, and the black arrows are for the impact of lithographic process variations. From Table 2, EGL method has about 2% underestimation for rising dealy and 2% overestimation for falling delay. Both rising and falling slews are overestimated by EGL. After considering SI_{EX} during device modeling parameter extraction, ON EGL methods for delay could be quite inaccurate and may mislead the design optimization.

As the same litho variation has different impact on PMOS and NMOS, its impact on timing issues of rising and falling are quite different, which are also shown in Table 2 & 3 with the title of "Our Model w/ V" which means lithographic variation is considered and simulated in our model.

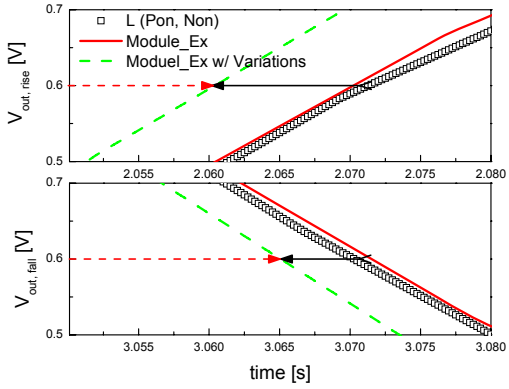

Fig.9 Rising and falling timing of V_{out}

Table 2 Output Delay Comparison

	Rising Delay		Falling Delay	
	(ps)	dif.	(ps)	dif.
Our Model	57.7	-	59.0	-
ON EGL	58.8	1.87%	57.8	-2.09%
Our Model w/ V	47.9	-17.0%	52.6	-11.0%

Table 3 Output Slew Comparison

	Rising Slew		Falling Slew	
	(ps)	dif.	(ps)	dif.
Our Model	124	-	110	-
ON EGL	125	1.18%	108	2.07%
Our Model w/ V	104	-16.2%	99.7	-9.47%

D. *Power Dissipated on the Post-Litho Cell*

Because dissipated power of the whole circuit not only directly impact power consuming, but also convert to thermal

issues and raise the temperature of the whole chip, power dissipation of the whole cell instead of the single device is study in this part. As the PMOS and NMOS alternatively play the role of the main character in the inverter cell, the power consuming of 1 dynamic and 2 static zones are analyzed as shown in Fig.10.

The comparison results are shown in Table 4 and 5. Table 4 compares the mean as well as peak dynamic power dissipation of two zones with different simulation methods and conditions. Table 5 is about static power dissipation on the cell. The most impressive result is that the static power/leakage simulation of OFF EGL may be seriously wrong (up to 56% overestimation). There are also obvious errors in other issues of both dynamic and static power consuming by any EGL.

The cell level simulation also shows that certain litho variation (defocus) are helpful to reduce total power consuming as average dynamic power can decrease by 10% to 20% (in Table 4), while static power only increase by just 0-2% (in Table 5). This is coincident to the common sense of gate length shrinkage. According to [14], depth-of-focus variations (no matter z is positive or negative) will induce decrease of gate length in this case. And the dynamic power of a single gate will be reduced as gate length shrinks [15]. And our unified post-litho device modeling card and circuit simulation can precisely simulate it.

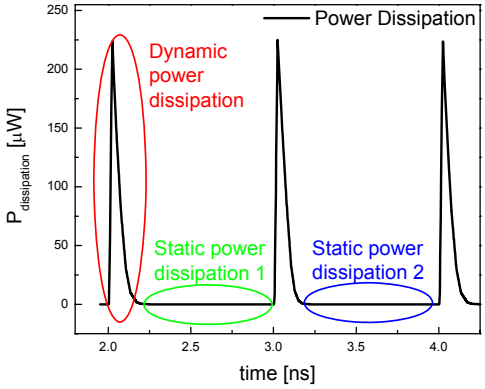

Fig.10 Power dissipation on the inverter

Table 4 Dynamic Power Dissipation

	Mean		Max	
	(μW)	dif.	(μW)	dif.
Our Model	41.13	-	223.7	-
ON EGL	42.68	3.79%	227.6	1.78%
OFF EGL	42.60	3.59%	247.6	**10.7%**
Our Model w/ V	33.56	**-18.4%**	211.9	-5.3%

Table 5 Static Power Dissipation

	Static 1		Static 2	
	(nW)	dif.	(nW)	dif.
Our Model	24.3	-	29.2	-
ON EGL	26.5	**9.05%**	31.1	**6.67%**
OFF EGL	62.2	**156%**	36.6	**25.3%**
Our Model w/ V	24.8	2.11%	29.2	-0.12%

VI. Conclusion

In this paper, a new non-rectangular device characterization and circuit simulation methodology is proposed using the drain-source current modification. The impact of nonrectangular gate shape during parameter extraction of device model (BSIM or PTM) is considered in the first time. Our model is validated and compared to the existing equivalent gate length (EGL) methodology. Our simulation results show that EGL methods may lead to serious errors on both timing estimation (2%) and leakage/ power estimation (up to 1.5X). Our non-rectangular model provides a unified and accurate extraction, characterization, and simulation flow for both timing and power. Given that nanoscale devices are becoming more and more non-rectangular, we expect our unified model be very useful for accurate timing and power analysis in future nanometer designs.

VII. Acknowledgment

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