Compact Modeling and Robust Layout Optimization for Contacts in Deep Sub-wavelength Lithography

Yongchan Ban and David Z. Pan
Department of ECE, The University of Texas at Austin, Austin, TX USA
ycban@cerc.utexas.edu, dpan@ece.utexas.edu

ABSTRACT

In this paper we propose a new equivalent contact resistance model which accurately calculates contact resistances from contact area, contact position, and contact shape. Based on the impact of contact resistance on the saturation current, we perform robust S/D contact layout optimization by minimizing the lithography variation as well as by maximizing the saturation current without any leakage penalty. The results on industrial $32nm$ node standard cells show up to 3.45% delay improvement under nominal process condition, 86.81% reduction in the delay variations between the fastest and slowest process corners.

Categories and Subject Descriptors

B.7.2 [**Hardware, Integrated Circuit**]: Design Aids

General Terms

Algorithms, Design, Performance

Keywords

Contact, Variation, Optimization, Lithography, DFM, VLSI

1. INTRODUCTION

The parasitic source/drain (S/D) contact resistance has been identified as a serious challenge and may ultimately limit device performance in nanometer devices [1, 2]. Previous works report that the variation of the contact area is the most critical problem in nanometer node devices [3, 4] because the contact area variation between the metal and silicide is mainly caused by manufacturing contact CD (critical dimension $\approx$ diameter) variation which results in the huge amount of change in contact resistance and performance degradation [3, 4].

As a result, there are many efforts on the analysis of S/D contact variation. According to [1, 2], the variation of the contact position causes a degradation of the saturation current in the stress induced device. This is because neighboring contacts may locally relax the actual strain in channel. Even though there are a lot of works on the variation of S/D contact resistance [1, 3, 4], none of them consider the impact of contact shape on the device performance. Therefore, it is in great demand to take all S/D contact variations (area, location and shape) into consideration. Although TCAD simulation can accurately calculate the impact of S/D contact variation, numerical methods are too slow and unsuitable for circuit level simulations. Thus a compact model for the geometric variations of S/D contact should be required. Moreover, both contact shape and area variations due to lithography process are highly related to the distance between contact layouts, which also affects the device stress in strained silicon CMOS. Those impacts lead to the optimization of S/D contact layout during design time.

In this paper, we propose the contact layout optimization considering both the device performance and the lithography process variation. Our approach is mainly based on the new spice level compact model for S/D contact layout. The objective of the proposed optimizations is to enhance standard cell layouts for improved parametric yield and reduced variations with minimal or no penalty on leakage and area constraints. Our major contributions include the following:

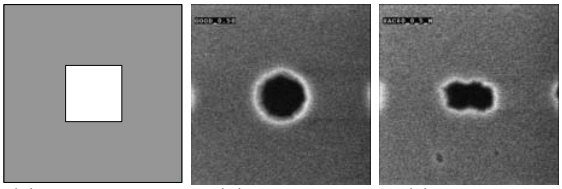
- We present the first systematic study on the impact of contact shape on the device saturation current, and propose a simple yet effective model to estimate the performance impact of S/D contacts. Our model considers contact distance from gate, contact shape, and contact area.
- We present an efficient contact optimization. In our formulation, we find the optimal contact position in a standard cell and achieve the best variability control by minimizing lithography process variation as well as the best performance by maximizing the saturation current without any leakage penalty.

The rest of the paper is organized as follows. Section 2 describes the sources of S/D contact variation and the timing impact. Section 3 presents the new compact model and its validation. Section 4 proposes the formulation and algorithm of the S/D contact layout optimization. Experimental results are discussed in Section 5, followed by conclusions in Section 6.

2. PRELIMINARY AND MOTIVATION

Printing of small geometries causes loss of image quality due to lithography proximity [6, 7], which results in distorted non-rectangular shapes of the geometries in S/D contact layer in Figure 1(b). If lithographic variations are added on lithography proximity in the contact patterning, the area variation of S/D contacts would be much more compared to the nominal process condition as shown in Figure 1(c).

Figure 2 shows the contact CD distribution at the nominal process condition (a) and the process variation (b) with the incremental contact pitch on the nominal $40nm$ contact. Let us assume in our paper that the the horizontal direction is



(a) Original mask (b) Proximity (c) Δ Process

Figure 1: Lithographic variations for contact [5]

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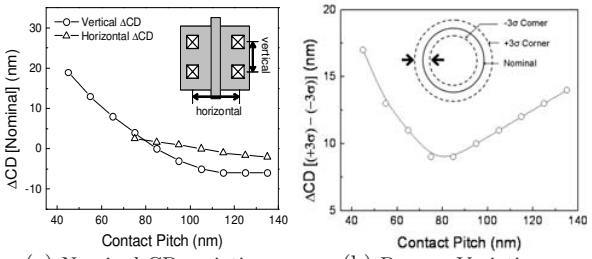
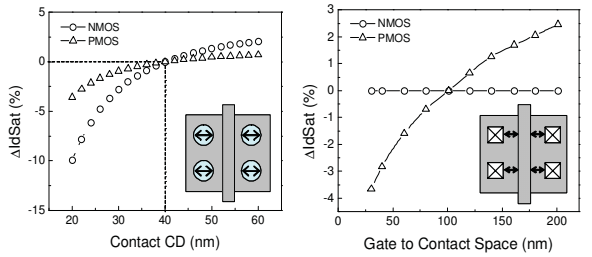


(a) Nominal CD variation (b) Process Variation

Figure 2: The lithographic contact CD variation.



(a) Area dependency (b) Position dependency

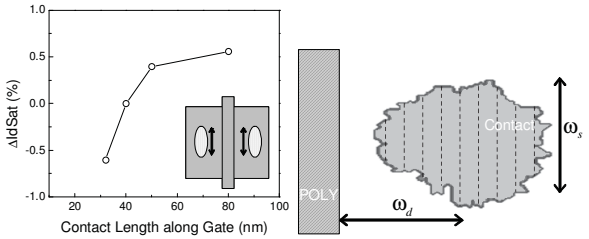
Figure 3: The impact of S/D contact variation

Electrically, the contact area variation is highly related to the device saturation current (I_{dSat}) degradation. As shown in Figure 3(a), we observe that $10nm$ contact CD variation causes up to 5% degradation of the saturation current, and the current variation is highly correlated with the contact CD variation. Figure 3(a) also shows that the current variation of NMOS due to the CD variation is more sensitive to that of PMOS because of the different resistance sensitivity.

The contact position also affects the saturation current in a device. According to the paper [1, 2], the variation of the contact position causes a degradation of the saturation current in the stress induced device. This is because neighboring contact hole may locally relax the actual strain in channel. As shown in Figure 3(b) [1], since the mobility modulation of PMOS is larger than NMOS, the saturation current degrades as contacts are placed closer to the gate in PMOS devices, meanwhile the current for NMOS shows almost no change. Although the current variation can be different from the stress parameters, we can find that the current variation by the stress relaxation due to the contact position could be different for NMOS and PMOS devices.

3. COMPACT S/D CONTACT MODEL

The lithography variation could vary the S/D contact shape, area and even distance from gate line, which causes the performance degradation as we see in Section 2. Thus, we should take the impact of S/D contact variation on the standard cell performance in design time, which needs a new circuit level compact model of S/D contact pattern.



(a) Shape dependency (b) Compact model

Figure 4: The impact of contact shape and a compact model

Sentaurus process and device simulator is used to estimate impacts of the contact effects on device performance, and to verify accuracy of the our compact model for non-rectangular contact layout. We first generate printed images of contact pattern with OPC taken into account. The standard cell layout is converted into 3D structure for TCAD simulation with Ligament layout editor. The $32nm$ CMOS cell uses intensive stress-enhancement techniques: NMOS uses a tensile stress liner, and PMOS has a compressive stress liner and embedded SiGe in S/D region.

To scrutinize the impact of contact shape, we test a set of contact patterns which have the same contact area but different contact shape under the TCAD simulation conditions. As shown in Figure 4(a), as the contact length along the gate line is larger, the saturation current is increased. This is because there is less current crowding from the S/D electric field and less stress relaxation of stress liner as the longest contact length is toward in the same direction with the gate.

As we can see in Figure 3 and 4(a), the saturation current due to the variation of S/D contact is highly dependent on the contact area, the horizontal distance from the gate line, and the contact shape along the vertical gate line. Since the saturation current is in inverse proportion to the contact resistance, we can consider the current impact of S/D contact by updating the S/D contact resistance. It implies that we get an accurate S/D contact resistance by exhibiting both the horizontal distance weighting factor and the shape weighting factor of the vertical direction.

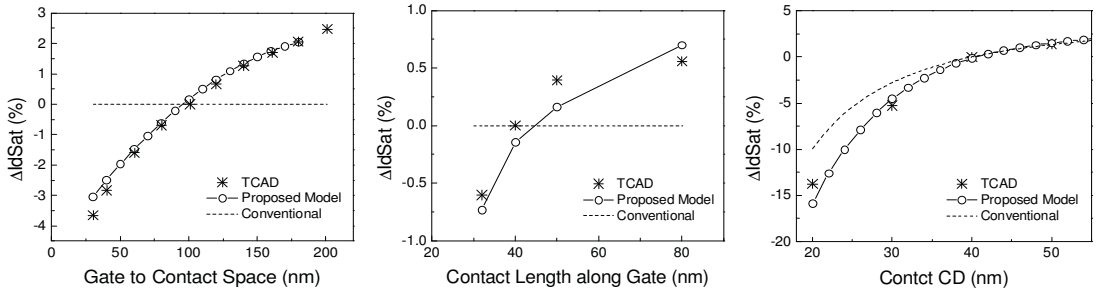
To estimate the current impact of contact resistance in a circuit level simulation, we propose an equivalent contact resistance model for various shapes of contact patterns. We first construct a set of look-up tables which include shape weighting factor, distance weighting factor for NMOS and PMOS S/D contact. Those two weighting factors are directly generated from the relations among the saturation current and the contact distance variation in Figure 3 and the contact shape variation in Figure 4(a), respectively. Once the printed images of contact holes are generated, we then classify NMOS contacts and PMOS contacts. Each contact is vertically sliced by a set of equal width polygons which keeps the original contact edge as shown in Figure 4(b). Then, we calculate a sliced polygon area and get a shape weighting factor (ω_s) and a distance weighting factor (ω_d). The weighting factors are directly related with the saturation current. Therefore, the weighting update can be done in O(1) access time.

Given i^{th} slice of a contact, the resistance of a sliced polygon is as follows:

$$R_i = \frac{\rho}{\omega_{d,i} \cdot \omega_{s,i} \cdot A_i} \quad (1)$$

where ρ is resistivity and A_i is the area of a slice. The equivalent of a contact is computed by summing all weighted areas of sliced polygons as following equation:

$$I_{dsSat} \propto \frac{1}{R_{co}} = \sum_i \frac{1}{R_i} = \frac{1}{\rho} \cdot \sum_i (\omega_{d,i} \cdot \omega_{s,i} \cdot A_i) \quad (2)$$



(a) Validation of Distance (b) Validation of Shape (c) Validation of Area

Figure 5: The impact of contact variation on the saturation current

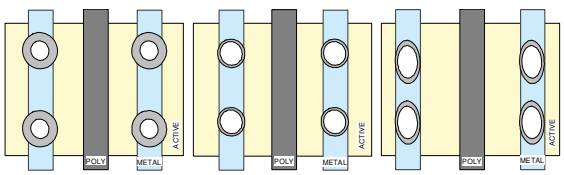
Since the total contact area can be a linear function of the number of contacts [1], the total weighted area is summated for all contact holes. The total resistance is calculated by dividing the resistivity (ρ) by the total weighted area. By applying this compact model, we can deal with any kind of contact shapes due to the lithography variations.

We validate our compact S/D contact model by comparing with an Sentaurus process/device simulation (TCAD) and Hspice simulation (Conventional). Note that the conventional circuit simulation just considers the contact area variation which is directly related with the contact resistance by dividing the contact resistivity by the contact area, meanwhile it is limited to analyze the contact shape and the contact distance effect due to device stress relaxation. Figure 5 proves that our contact resistance model is well matched with TCAD results in terms of the distance from the PMOS gate (a), the contact shape (b), and the contact CD (area) of NMOS (c). The reason why our model matches with the TCAD results is that we use the contact distance and shape weighting look-up tables which are generated from accurate TCAD simulations. The overall 0.16% current error in the contact shape is due to the fact that we linearly sum up the contact shape weighting factor of each sliced contact polygon, and the all of sliced polygons in a contact have different distance from the gate line.

4. CONTACT LAYOUT OPTIMIZATION

From Figure 3, even though the sensitivity of contact variation could be different from input process condition, this tells us that the optimal position of NMOS and PMOS contact holes might be different for the best printability and device performance in standard cell. Thus, we should find the optimal S/D contact layout in design time by taking the process variability due to lithography and the performance dependency due to stress relaxation into consideration.

The lithography may cause a huge amount of contact CD (area) and shape variation in a standard cell. These variation is highly related to the S/D contact position which also affects the channel stress. Since contact patterning is prone to lithography proximity and process variations, the robust design from the lithography process variation is desirable for S/D contacts in a cell. Thus the contact printability is one of key concepts in our layout optimization. In device performance point of view, the main goal of S/D contacts is to provide enough current to devices from the voltage source. The longer vertical length of contact pattern induces the higher devices performance as shown in Figure 5. Thus, we can consider the S/D channel current friendly design of contact which is achieved by adjusting the S/D contact space.



(a) Conventional (b) ΔPV-best (c) I_{dSat}-best

Figure 6: S/D contact layout optimization

Therefore, we can optimize the S/D contact layout as following categories:

Variability-driven Design We optimize the contact layout by minimizing the contact CD variation due to lithography process given the device performance tolerance. As shown in Figure 6(b), the main goal is to minimize the contact CD variation between the fastest and slowest process corners by finding the best position of the contact pattern.

Performance-driven Design In the range of process variation tolerance, we optimize the contact layout by maximizing the saturation current. Generally, the contact CD increases as the pitch decreases. Thus we can make vertically long contacts by reducing the space between contacts as shown in Figure 6(c).

As shown in Figure 2, the printability of S/D contacts is highly dependant on the contact pitch. Although the optical conditions for S/D contact patterning might be different from contact design, the contact patterning follows a similar CD trend where the CD variation due to process variation has the minimal value [9], and where the contact layout is the most robust from the lithography process variation. In addition, the impact of device stress is similar to Figure 5(a) in spite of different stress mobility of NMOS and PMOS devices. Therefore, from the results of Figure 5 and 2, we can mathematically formulate a contact optimization problem with *the minimal process variability* as follows:

$$\begin{aligned} \textbf{min}: \quad & \Delta PV \\ \textbf{s.t.}: \quad & I_{th} \leq I_{dSat} \\ & \Delta I_{dSat} = f_{hd}(x),\ \Delta PV = f_s(y) \text{ given design rule} \end{aligned} \tag{3}$$

The objective is to minimize the process variation (ΔPV) between the $+3\sigma$ corner and the -3σ corner of lithography process as shown in Figure 2(b), and the constraint is to keep the saturation current I_{dSat} to be more than a given current tolerance I_{th}. This constraint can be expressed as $\Delta I_{th} \leq \Delta I_{dSat}$, where ΔI_{th} is a negative value. The formulation $f_{hd}(x)$ is the function between the horizontal distance of S/D contacts from Figure 5(a), and $f_s(y)$ is the function of process variation from Figure 2(b), respectively. The variable x means the horizontal direction, meanwhile the y means the vertical direction in a cell. The contact variation due to process variation is highly dependent on the vertical contact distance which determines the contact shape and the process robustness of contacts. Meanwhile the nominal CD variation is related to the horizontal contact distance which impacts on the contact CD and device stress.

In this formulation, we assume that the horizontal optimization of contact holes is mainly driven by the device stress effect, and the vertical optimization is controlled by the lithography proximity and variation. These assumptions are reasonable because: (1) the horizontal CD variation due to lithography variation is much less than the CD variation of the vertical direction, (2) the stress relaxation due to the contact holes is mainly caused by the distance between gate and contacts (vertical direction). The $f_{hd}(x)$ and $f_s(y)$ are both convex, which enables to solve the formulation in

Table 1: Improvement of Delay

Cell	Original Design			Variability-driven Design						Performance-driven Design					
	FF[a]	Norm[a]	SS[a]	FF	%[b]	Norm	%	SS	%	FF	%	Norm	%	SS	%
INVX5	17.77	18.04	19.65	17.51	1.44	17.84	1.12	17.91	8.85	16.73	5.82	17.71	1.88	18.31	6.83
NAND2X2	24.53	24.63	26.46	24.39	0.56	24.42	0.83	24.64	6.86	23.20	5.43	24.44	0.76	25.18	4.83
NOR2X2	32.31	32.65	34.34	31.99	0.98	32.22	1.34	32.31	5.92	30.83	4.58	32.05	1.84	32.54	5.27
AND2X2	56.18	57.83	59.86	55.66	0.91	56.55	2.21	57.92	3.24	54.96	2.16	55.91	3.32	57.50	3.95
HA_S	138.50	142.32	147.55	137.27	0.89	139.43	2.03	142.06	3.72	135.62	2.08	137.81	3.17	141.07	4.39
HA_C	76.89	79.37	82.79	76.29	0.78	77.72	2.07	79.43	4.06	75.24	2.15	76.63	3.45	78.91	4.69
FA_S	305.96	312.89	322.10	303.24	0.89	307.02	1.88	312.15	3.09	300.31	1.85	304.32	2.74	310.65	3.56
FA_C	244.10	249.04	255.90	242.25	0.76	244.71	1.74	248.53	2.88	240.06	1.66	242.93	2.46	247.23	3.39
average					0.90		1.65		4.83		3.22		2.45		4.61

[a] FF: -3σ process corner. Norm: nominal process condition. SS: +3σ process corner. The unit of delay is ps.
[b] It represents the improvement of the cell delay. We compared all delay value with the original design.

polynomial time and to find the globally optimal position of contacts with minimal manufacturing variation [10].

If the amount of lithography process variation is allowed, we can find the optimal contact position with *the maximal device performance*. The formulation is as follows:

$$\textbf{max}: \quad I_{dSat} \tag{4}$$
$$\textbf{s.t.}: \quad |\Delta CD| \leq |\Delta CD_{th}| \ \& \ |\Delta PV| \leq |\Delta PV_{th}|$$
$$\Delta I_{dSat} = f_{vd}(y), \ \Delta CD = f_{cd}(y) \text{ given design rule}$$

The objective is to maximize the device saturation current, and the constraint is that the lithographic process variation should be less than the given process tolerance ΔPV_{th} and the nominal CD variation also should be less than the given CD tolerance ΔCD_{th}. The formulation $f_{vd}(y)$ is the current impact due to the vertical contact distance from Figure 5(b), and $f_{cd}(y)$ is the contact CD variation from Figure 2(a), respectively. The vertical longer contact CD is preferable for the better device performance. Since the functions $f_{vd}(y)$ and $f_{cd}(y)$ are convex, we can obtain the globally optimal position of contact holes for the maximal device performance.

5. EXPERIMENTAL RESULTS

We implemented the compact S/D contact resistance model and the contact layout optimization in Tcl and Perl script language and tested with the industrial 32nm standard cell. The nominal contact size is 40nm for all standard cells. In order to model and solve the convex formulation, we used AMPL/MOSEK 5.0. After calculating the effective S/D contact resistance, we updated the value in netlist file and measured the current and the delay using Hspice. We used Calibre-WB for model based OPC and printed images.

The current improvement results in the delay reduction in a standard cell. Table 1 compares results from the two design optimization approaches: the variability driven optimization and the performance driven optimization. We measured the three delay values for different S/D process variations: -3σ process corner (FF), nominal process condition (Norm), and +3σ process corner (SS). It shows that we improve overall delay and delay variation by adjusting the contact position. The results shows up to 3.45% delay improvement and 2.45% improvement of averaged delay under nominal process condition. The 3.45% delay improvement by the S/D contact optimization is equivalent to about 8% reduction of gate length for faster speed without any leakage current. The leakage current variation is shown in Table 2. Therefore the impact of contact optimization on the delay is substantial. True to our expectation, the delay reduction in the performance-driven optimization is higher than that of the variability-driven optimization.

In Table 2, we compared the delay variation which represents the delay difference between the -3σ process corner and +3σ process corner. As shown in Table 2, the results shows up to 86.81% reduction of the cell delay in the variability-driven design and up to 37.80% reduction in the performance-driven design. Even though the delay reduction of the variability-driven design in the nominal process condition is somewhat smaller than the performance-driven design as shown in Table 1, yet the variability-driven design shows much more improvement in the decrease of the delay variation between the fastest and slowest process corners.

Table 2: Improvement of Delay Variation

Cell	ORG[a]	VAR[a]		PERF[a]		leakage
(%)	ΔD	ΔD	Imp[b]	ΔD	Imp[b]	ΔI_{off}
INVX5	10.43	2.23	78.61	8.89	14.77	0.00
NAND2X2	7.83	1.03	86.81	8.11	-3.62	0.00
NOR2X2	6.23	0.99	84.18	5.32	14.63	0.00
AND2X2	6.38	3.99	37.39	4.54	28.84	0.00
HA_S	6.36	3.44	45.95	3.96	37.80	0.00
HA_C	7.44	4.04	45.68	4.80	35.49	0.00
FA_S	5.16	2.90	43.74	3.40	34.17	0.00
FA_C	4.74	2.57	45.86	2.95	37.67	0.00
average			58.53		24.97	

[a] ORG: Original design. VAR: Variability-driven. PERF: Performance-driven.
[b] Improvement from the Δdelay of original design.

6. CONCLUSION

We have proposed a novel contact equivalent resistance model and layout optimization approach in standard cell library to minimize the lithography process variation as well as to maximize the saturation current within process tolerance. Experimental results with a industrial cell library show that our model-based contact layout optimization approach can substantially decrease the delay and variation given layout constraints.

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