Accurate Power Grid Analysis with Behavioral Transistor Network Modeling

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Motivation

Power grid analysis rely on a model of representing the transistor network as a current source (CS).

- This simplification enables decoupling the transistor network from the power grid.
- The power grid problem becomes tractable due this simplification.

But CS modeling might lead to pessimism in the voltage drop prediction.

- Does not accurately model transistor load cap
Current Source Modeling

- Current source models switching gates
  - Also drain cap of a gate (not shown) is modeled approximately
- The power grid problem mathematically reduces to solving a linear system of equations $Ax = b$.
  - Efficient techniques to solve it
Drawbacks of Current Source Modeling

- When a transistor switches on and connects to the power grid, *initially* the charge is supplied by the transistors that are already on.
  - The transistors which are already on, act much like a “decap”
  - Need accurate modeling of load cap of gates
    - Inaccurate modeling results in the overestimation of decap needed.

- The number of transistors that get switched on differs from cycle to cycle.
  - Thus the amount of capacitance seen by the power grid also varies from cycle to cycle.
Literature

- Chen-Neely [IEEE T-CPM, 1998]
  - Modeling techniques to analyze power grid
  - Current source model to decouple transistor network from power grid

- Lot of work on solving linear system of equations arising out of power grid analysis
  - Preconditioned Krylov [Chen and Chen, DAC 2001]
  - Random-Walk [Qian-Nassif-Sapatnekar, DAC 2003]
Switch model for transistors

Switch Model of a transistor [Horowitz 1983]
- Originally proposed to calculate the delay of transistor
- Accurately models capacitance of every transistor in the gate
- Correctly models the time varying capacitance
The major disadvantage of the switch model is, based on whether the switch is *on* or *off*, the topology changes.

**A_{open}**

\[
\begin{pmatrix}
1 & 0 \\
0 & 1/R_2
\end{pmatrix}
\begin{pmatrix}
V_1 \\
V_2
\end{pmatrix} =
\begin{pmatrix}
V_{dd} \\
0
\end{pmatrix}
\]

**A_{close}**

\[
\begin{pmatrix}
1 & 0 \\
-1/R_1 & 1/R_1 + 1/R_2
\end{pmatrix}
\begin{pmatrix}
V_1 \\
V_2
\end{pmatrix} =
\begin{pmatrix}
V_{dd} \\
0
\end{pmatrix}
\]
Problems with Switch Modeling

- Conductance matrix \((\mathbf{A})\) changes with the state of the switch
  - \(\mathbf{A}_{\text{open}} \mathbf{x} = \mathbf{b}\)
  - \(\mathbf{A}_{\text{close}} \mathbf{x} = \mathbf{b}\)

- Modeling \(k\) transistors leads to \(2^k\) different conductance matrices.
  - \(k = 10 \Rightarrow 1024\) different conductance matrices
  - Infeasible even for a complex gate!

- Thus we need a constant conductance matrix irrespective of the state of the switches.
Behavioral Model of a Switch

In $Ax = b$, instead of capturing switch position in $A$ can we capture it in $b$? 
- Model the switch behaviorally

The behavior of the ideal switch ($s$) is very simple:

$s = \text{open} \Rightarrow i_s = 0$

$s = \text{close} \Rightarrow v_s = 0$

The behavioral modeling helps capture the state of switches in $b$ ($Ax = b$) 
- Results in constant conductance matrices irrespective the state of switches
Example of behavioral model of switch

Applying Kirchhoff’s law we get

\[- V_{dd} - v_s + i_s (r_s + R_1 + R_2) = 0\]

To emulate the behavior of switch

- Open: \( i_s = 0 \Rightarrow \text{Set } v_s = -V_{dd} \)
- Close: \( v_s = 0 \)
Constant conductance matrix

Since only the value of the voltage source changes the topology does not change

\[
\begin{pmatrix}
1 & 0 & 0 & 0 \\
-1 & 1 & 0 & 0 \\
0 & -1/r_s & 1/r_s+1/R_1 & -1/R_1 \\
0 & 0 & -1/R_1 & 1/R_1+1/R_2
\end{pmatrix}
\]

Only \( v_s \) depends on the state of the switch
- Hence conductance matrix is a constant irrespective of the state of switches
A bit history of behavioral switch model

More formally the switch model is called the Associated Discrete Circuit (ADC) model

Developed independently by two groups:
- Hui and Morrall (University of Sydney, Australia)
- Pejović and Maksimović (University of Colorado, Boulder)
- Both of the groups were motivated by the switching power system simulations
  - Papers published in 1994
Current source based ADC for switch

- Current source based ADC is more suited to simulation compared with voltage source based ADC.
- In a MNA formulation:
  - Current Source does not need a separate row in conductance matrix.

To emulate the behavior of switch:
- Open: Set $j_s = -i_s$
- Close: Set $j_s = 0$
Theorem: the resultant conductance matrix is a $\mathcal{M}$-matrix

Lot of efficient algorithms for solving $\mathcal{M}$-matrix
- Preconditioned Krylov [Chen-Chen DAC 2001]
- Multigrid methods [Kozhaya-Nassif-Najm TCAD 2002]

Thus algorithms previously presented in the literature for power grid analysis can be applied to our new model without much change.
Phases in power grid simulation

- **Local charge redistribution phase.**
  - When the transistor gets switched on to the power grid, the charge is supplied by the local capacitors.

- **Global recovery phase.**
  - Bringing capacitors back to their original state
Speedup Techniques

- **Local charge redistribution phase**
- Time-step is decided by the fast transients
  - To track them accurately, the time-step has to be small
  - When the power grid recovers back after this fast transient voltage drop the time-step can be big
- Can we calculate this voltage drop using a fast approximation without doing a detailed simulation?
  - Then we can use a bigger time-step in rest of the simulation.

- **Use the Principle of Locality** [Zhao-Roy-Koh TCAD 2002]
  - **Drawback**: Applies only if the switching events are isolated
Speedup Techniques

Global recovery phase

Once grid recovers back to the supply voltage in a given cycle it is going to stay at the supply voltage.

Thus the power grid simulation can be fast-forwarded to the start of the next cycle.
Experiment setup

- Scripts were written using awk/perl/matlab
- The experiments were done using a 32-bit Linux machine with 4 GB RAM and running at 3.4 GHz
- The delay models were generated using the 90nm Berkeley Predictive Technology Model
- While solving $Ax = b$ we employed simple LU factorization
  - Used Approximate Minimum Degree (symamd) reordering on $A$ to obtain sparse $L$ and $U$
The error in voltage drop predicted by current source model for ckt9 compared to ckt1 is bigger.

- In ckt9, there are more transistors hooked to the power grid node compared to ckt1.
- Decoupling capacitance provided by the transistors which are on, is much bigger in ckt9 compared to ckt1.

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<th>Error [%]</th>
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Summary

- We analyzed the power grid by modeling the transistor network accurately by switch models instead of a time-varying current source.
- The transistor is modeled as a simple switch in series with a RC circuit.
  - The switch is modeled behaviorally as a Norton current source model.
  - The behavioral modeling of the switch is the key in making the proposed simulation efficient.
- More accurate compared to the current source model.
  - Also retains the efficiency of current source model by having a constant conductance matrix.
Conclusions

- Proposed a behavioral model for transistors in the context of power grid analysis.

- The proposed model offers the middle ground between the accuracy of SPICE simulation and the speed of the current source model.

- Working on fast approximation methods to find the voltage drop in the local charge redistribution faster
  - This will help to improve time-step and hence the runtime.
Thanks