# ELIAD: Efficient Lithography Aware Detailed Routing Algorithm With Compact and Macro Post-OPC Printability Prediction

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***Abstract*—In this paper, we present an efficient lithography aware detailed (ELIAD) router to enhance silicon image after optical proximity correction (OPC) in a correct-by-construction manner. We first quantitatively show that a pre-OPC litho-metric is highly uncorrelated with a post-OPC metric, which stresses the importance of a post-OPC litho-metric for design-time optimization. We then propose a compact post-OPC litho-metric for a detailed router (DR) based on statistical characterization, where the interferences among predefined litho-prone shapes are captured as a lookup table. Our litho-metric derived from the characterization shows high fidelity to the total edge placement error (EPE) in large scale, compared with Calibre OPC/optical rule check. Therefore, ELIAD powered by the proposed litho-metric can enhance the overall post-OPC printed silicon image. Experimental results on 65-nm industrial circuits show that ELIAD outperforms a rip-up/rerouting approach such as Resolution-enhancement-technique-Aware Detailed Routing with 8× more EPE hot spot reduction and 12× speedup. Moreover, compared with a conventional DR, ELIAD is only about 50% slower.**

***Index Terms*—Algorithm, lithography, manufacturability, printability, routing, synthesis.**

## I. Introduction

NANOMETER VERY large scale integration (VLSI) design is facing grand challenges from manufacturing limitations which include the printability issues due to sub-wavelength lithography [4], [15], [17], [21], [26], the topography variations due to chemical–mechanical polishing [5], [9], [11], [25], the random defects due to missing/extra material [6], [18], [22], the via failure [3], [19], [27], and so on. In the nanometer regime, thus, we need to ensure not only conventional design (e.g., timing, power, and noise) closure but also manufacturing closure. As it has been shown that manufacturing issues are strongly layout dependent, manufacturability aware layout optimization for manufacturing closure shall play a critical role in the overall yield improvement.

Among multiple manufacturing issues, lithography with 193-nm wavelength is one of the most fundamental challenges due to its impact on yield and timing, and expected to be more serious in advanced technologies. Even worse, as of now, the 193-nm (wavelength) optical lithography is still the dominant IC manufacturing process for 65- and 45-nm nodes, and next-generation lithographies are not likely to be in the mainstream in the near future [20]. Accordingly, major IC manufacturers will continue to use the current 193-nm lithography to print 65, 45, and 32 nm and below, heavily relying on resolution enhancement techniques (RETs) such as optical proximity correction (OPC).

OPC modifies GDSII for better printability as a post-tape-out mask synthesis and becomes a crucial manufacturing step in sub-90-nm designs but at a cost of high computational complexity, as well as soaring mask cost. Nevertheless, OPC may be too late to make all the necessary corrections due to restricted design flexibility. These drawbacks of OPC put lithography aware design [as a part of design for manufacturability (DFM)] in greater demand than ever, so that the downstream lithography and OPC effects can be abstracted and estimated for better design decisions in terms of manufacturability and yield.

As a result, there are many manufacturability aware efforts in earlier design stages such as logic synthesis and placement [10], [14], but routing is often believed to be one of the most important stages to address the lithography issues due to the following reasons [15], [21]: **1)** Wire printability is coupled with interconnection network which is mainly determined by routing; **2)** routing is the last major VLSI physical design step before manufacturing, thus having more comprehensive and accurate information on lithography; and **3)** routing still has considerable design flexibility to find reasonable tradeoffs between printability and conventional design objectives (e.g., timing, noise, and power). These factors lead to a lot of recent academic and industrial efforts in *lithography aware routing*, particularly detailed routing, owing to the small influence window of optical lithography.

One easy approach for lithography aware routing would be to introduce manufacturability aware rules, but such rule-based approaches suffer from an exploding number of rules, expensive rule checking, and, more importantly, large area/timing overhead due to over guard band. These limitations lead to

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several model-based approaches. The first OPC aware maze routing in [15] is based on multiconstrained shortest path (MCSP) optimization with a subgradient method. A multilevel routing approach to minimize the number of OPC features is studied in [4]. As postoptimization, rip-up/rerouting (RR) approach to remove litho hot spots is proposed based on fast lithography simulation [21] or pattern matching [17]. However, there are a few drawbacks in these prior works: **1)** Printed or silicon image is not directly addressed [4], [15]; **2)** the result is not verified with an industrial sign-off tool under inevitable defocus [4], [15], [21]; **3)** the burden of trivial litho hot spots which can be easily fixed by OPC is imposed on router by ignoring OPC [21]; and **4)** postoptimization inherently cannot make radical changes enough to address lithography issues [17], [21].

In this paper, we propose an efficient lithography aware detailed (ELIAD) router based on a compact and high fidelity post-OPC litho-metric. Our litho-metric shows high correlation ($> 0.95$) to total edge placement error (EPE) computed by Calibre OPC/optical rule check (ORC) in large scale. We plug this metric into ELIAD using Lagrangian relaxation. The major contributions of this paper include the following.

1) We show that a pre-OPC litho-metric is not accurate enough to guide design-time printability enhancement.
2) We propose a compact and high fidelity litho-metric with OPC taken into account. Our metric is from statistical weak grid (WG) characterization which has several advantages over pattern characterization.
3) We present an ELIAD router to optimize post-OPC silicon image. In our formulation, we adopt the proposed litho-metric in ELIAD by applying a Lagrangian relaxation technique.
4) We propose a technique for fast convergence of subgradient optimization, using WG shadowing around blockages and routed nets.
5) ELIAD is the first lithography aware detailed router (DR) targeting post-OPC image in a correct-by-construction fashion. Routing results are verified with an industrial ORC under a realistic OPC recipe.

The rest of this paper is organized as follows. Section II provides preliminaries on lithography. In Section III, we present a comprehensive survey on lithography aware routing. Section IV compares pre- and post-OPC litho-metrics. Our litho-metric is described in Section V. Section VI proposes ELIAD. Experimental results are discussed in Section VII, followed by conclusion in Section VIII.

## II. Preliminaries

To fill up the gap between rapidly shrinking feature size and optical wavelength, several RETs are applied in advanced technologies such as OPC, phase mask shifting, off-axis illumination, and so on. Among them, OPC is one of the most widely used RETs, which modifies layout patterns to improve printability [24]. Fig. 1 shows an example of OPC by contrasting silicon images with and without OPC. Since OPC is not optional in 90 nm and below, it is essential to consider in any lithography aware design optimization the limitations of OPC (whether a hot spot can or cannot be fixed by OPC) [28], [29].

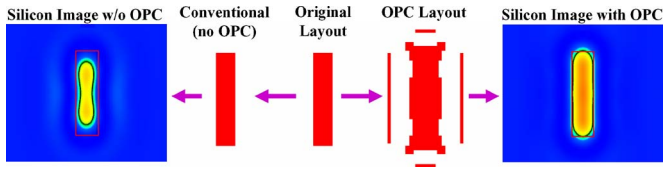


Fig. 1. OPC example [15].

In optical lithography, EPE is measured as the difference between target and printed contours. EPE is a popular concept to adjust the polygon edge during OPC and can be used to measure the quality of layout in terms of printability [21]. Accordingly, a litho hot spot can be defined as a spot where EPE is larger than a given critical dimension (CD) tolerance and detected by ORC.

## III. Previous Works

Optical projection systems in modern optical lithography technology usually use partially coherent illumination. Since a partially coherent system can be approximately decomposed into a small number of $P$ fully coherent systems [15], [23], the aerial image intensity $I(x, y)$ at the point $(x, y)$ can be shown as follows by approximating Hopkins equation [2] through the kernel decomposition [7]:

$$I(x,y) = \sum_{i=0}^{P-1} \left| \sum_{j \in W(x,y)} (F_j \odot K_i)(x,y) \right|^2 \quad (1)$$

where $K_i$ is the transfer function for the $i$th fully coherent optical subsystem, and $F_j$ is the transmission function (one and zero over clear and opaque regions, respectively) of the $j$th rectangle in effective window $W(x, y)$. The size of the $W(x, y)$ depends on the wavelength and numerical aperture (NA) of the optical system but, in general, is about 1–4 $\mu$m. Based on (1), lithography simulations can be performed to obtain aerial images and then printed silicon images.

The first attempt to address the lithography problem in routing is the OPC aware maze routing work in [15]. Based on aerial image simulation, it stores the expected OPC cost in a lookup table, which has the information on the interference from patterns at different lengths by distance. While routing a new pattern, the interferences from all existing patterns in its influence window are looked up from the table and then summed up to evaluate the total optical interference from existing patterns. Meanwhile, the optical interference (OPC cost) on the existing patterns due to the new pattern is estimated as the maximum interference on these patterns. Then, a vector-weighted graph method is applied to map the grid routing model to a graph, where the edge cost is a vector consisting of the interferences from the existing patterns, as well as the interference of a new pattern to the existing patterns. With such vector-weighted graph, OPC aware maze routing can be cast as an MCSP problem, which is then solved by Lagrangian relaxation. Note that optical interference is not a direct litho-metric, while the EPE that is widely used in OPC algorithms is.

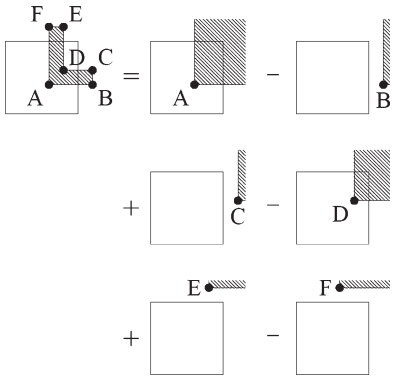


Fig. 2. Convolution lookup for fast lithography simulation [30].

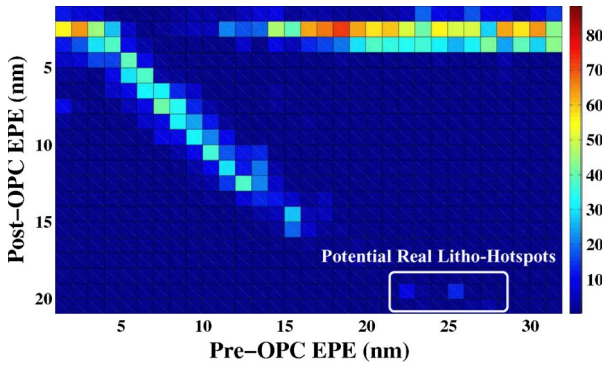


Fig. 3. This plot shows how a pre-OPC EPE distribution will be mapped to a post-OPC EPE distribution. From this result, we can conclude that most pre-OPC EPE hot spots will be taken care of by OPC algorithms. Therefore, a lithography aware detailed router should use a post-OPC EPE metric to capture real litho hot spots rather than to optimize trivial easy-to-fix-by-OPC hot spots with design overhead (e.g., wire length, run time, via, and so on).

Another lithography aware maze routing algorithm is proposed in [26], where a table of electric amplitude of diffraction (EAD) is prebuilt, and the OPC error is estimated as the square of the accumulated EAD values from the patterns within a process window. Then, it greedily performs maze routing such that a routed path for each net exceeds neither OPC error threshold nor path length constraint. Again, it shall be noted that the EAD square metric is not a direct/verified lithography measurement.

The RET-Aware Detailed Routing (RADAR) work [21] is the first attempt to directly link a lithography simulator (using the direct EPE) to the detailed routing. Based on fast lithography simulation techniques which are more suitable for full-chip simulations, it generates the so-called lithography hot spot maps to guide the postrouting optimization, namely, wire spreading and RR. As an example to measure the lithography and RET effort, the EPE metric is used. To compute EPE efficiently, [21] relies on effective kernel decomposition method and fast table-lookup techniques. In the kernel decomposition-based simulation, a core computational step is the convolution term. Due to the linearity of convolution in (1), the convolution for any arbitrary rectangle inside the effective window can be decomposed into four upper-right rectangles, which can reduce the table size significantly [21], as shown in Fig. 2. After the litho hot spot map is obtained from fast lithography simulations, wire spreading and RR can be applied to reduce the EPE hot spots and improve printability. The fast lithography simulator is called during the routing modification if needed to make sure that no new lithography hot spots occur. The result implies that both wire spreading and RR are effective in reducing EPE hot spots, but RR can be more effective than wire spreading with less wire length overhead.

Similar RR approach is proposed in [17], but effective pattern searching instead of litho simulation is adopted, i.e., a set of known undesirable patterns is stored/matched to identity litho hot spots. Then, the identified undesirable routing patterns are either removed or modified by performing RR. Recently, a multilevel routing approach to minimize the number of OPC features is studied in [4]. A simple OPC cost, which becomes higher for longer and wider wires, is proposed and applied as a factor in maze routing. It shall be noted that the lithography aware routing is still in its infancy, and there are many research issues to achieve holistic understanding for it.

## IV. Pre- and Post-OPC EPE Comparison

In all the previous papers in Section III, the lithography optimization is performed based on pre-OPC metrics. However, considering the strength of industrial OPC algorithms/tools, pre-OPC metrics can significantly misguide optimization. To understand the correlation between pre- and post-OPC EPEs, as well as the performance of the state-of-the-art OPC, we collect 0.5 million sampling locations from a 65-nm industrial design. Please see Section VII for details. Fig. 3 shows the correlation by plotting how pre-OPC EPE (on the $x$ axis) can be mapped to post-OPC EPE (on the $y$ axis). Overall, it shows that an industrial strength OPC algorithm can effectively reduce EPE, resulting in no correlation between pre- and post-OPC EPEs ($R = -0.36$). In particular, it shows an impressive performance in optimizing the litho hot spots with relatively large pre-OPC EPEs (e.g., $> 15$ nm), eliminating most of the hot spots. However, a small number of such pre-OPC litho hot spots remain as real post-OPC litho hot spots even after OPC, as shown in Fig. 3. As no litho hot spot is allowed for chip tape out, such post-OPC litho hot spots should be fixed through design modification. The result in Fig. 3 leads to several key observations for lithography aware design optimization, stressing the criticality of a post-OPC EPE metric as follows.

1) Since an advanced OPC algorithm is highly effective in improving printability, optimizing pre-OPC litho hot spots during design time can incur unnecessary design overheads in terms of wire length, timing, noise, and so on.
2) As OPC is a must step in sub-90-nm nodes, design-time lithography optimization should focus on real post-OPC litho hot spot elimination.

We further analyze the patterns of post-OPC litho hot spots and find out highly frequent appearance of singular grids (e.g., line end, jog corner, via, and so on) around such hot spots. There are two intuitive explanations behind this finding: **1)** OPC algorithms cannot converge efficiently, when there are multiple singular grids in a process window, and **2)** OPC recipes are tuned for the most common case, which is two paralleled running wires. This observation leads to the characterization of

such cases, which becomes one of the key ideas in our post-OPC printability metric in Section V.

## V. Post-OPC Printability Prediction

In this section, we present our litho-metric to predict post-OPC printability during detailed routing. The focus of our metric is to estimate the impact of a routing decision on *global* (large scale) printability fast enough, so that it can be leveraged as a part of a DR. We intend to neither compute the exact EPE of a certain spot nor identify litho hot spots accurately. We are mainly interested in guiding a router to generate more litho-friendly layout by capturing global *trend* at small cost. In this aspect, our metric is different from another fast hot spot detection using graph in [16] and is more suitable for a DR.

The motivation behind OPC consideration in our metric is that a pattern which is believed to be litho *unfriendly* can be printed successfully, depending on OPC algorithms and recipes. Considering OPC as an essential step, a litho-metric or fast lithography simulation [21], [29] without OPC can burden a DR unnecessarily by blindly optimizing some easy-to-fix-by-OPC litho hot spots.

In Section V-B, we propose our litho-metric using the statistical WG-type (WGT) characterization in Section V-A. Section V-C shows the high fidelity of our metric.

### A. Statistical WGT Characterization

In industry, pattern matching has been done to identify litho-unfriendly patterns, so that it can be used in postptimization for litho hot spot removal. Moreover, it can yield very accurate hotshot detection, if a pattern library is comprehensive enough. However, pattern matching is inefficient in guiding a DR in a correct-by-construction manner due to the following reasons.

1) **Run time.** Pattern matching is computationally too expensive to be used in a DR even with the latest algorithm [28], [29], as detail routing is already one of the slowest steps in VLSI design.
2) **Memory.** Depending on technology, the number of patterns we need to store can explode. Therefore, it may consume too large memory for an already-memory-hungry DR.
3) **Update.** Whenever there is a change in either process technology or OPC recipe, pattern characterization needs to be redone to reflect the latest fab condition. However, the characterization for pattern matching requires long time and huge efforts due to a large number of possibilities.
4) **Decomposability.** Pattern matching cannot be done incrementally due to the lack of decomposability. Any change in layout should invoke new pattern matching, as the change cannot be decoupled from the original layout. Considering heavy RR in a DR, pattern matching is not efficient.

Therefore, we propose a simple yet effective grid-based statistical characterization scheme based on the following definitions:

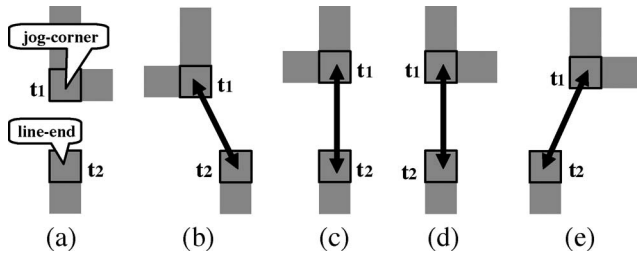


Fig. 4. WGT characterization for $t1 = jog\ corner$ and $t2 = line\ end$ is shown, where (b), (c), (d), and (e) are the cases with the same distance. Thus, the mean EPE will characterize this interaction between $t1$ and $t2$ at this distance.

- WG is defined as a detailed routing grid filled with one of the predefined litho-prone shapes.
- WGT is defined as the type of the litho-prone shape embedded on the corresponding WG.

Note that a detailed routing grid is the routing granularity used in detailed routing algorithm: It physically means a small polygon which can be filled up with metal from a minimum width wire or left unused for minimum spacing. Fig. 4(a) shows an example of two WGTs, which are a jog corner and a line end. Based on given predefined shapes which are highly prone to lithography or CD variation, the interference between WGTs is captured statistically.

We describe our statistical WGT characterization in Algorithm 1. The first input is a set of WGT $T$. The second input is the maximum distance at which two types from $T$ can interfere. Then, as in line 5, we enumerate multiple patterns w.r.t. two types at various distances to see the relation between distance and a pair of WGTs. After performing lithography simulation for each pattern as in line 8, we compute a mean EPE for a triple which consists of two WGTs and distance as in line 13. While computing the mean, we ignore noise/minor EPE hot spots (in our case, $\leq$ 5 nm) as in line 9. Hence, the mean EPE statistically represents printability as a function of distance. Fig. 4(b)–(e) shows some example patterns with the same distance between the jog corner and the line end.

**Algorithm 1 Statistical WGT Characterization**
**Require:** A set of WGT $T$, a max distance $d$
1: Table WGT_TABLE $\leftarrow \emptyset$
2: **for** each type $t1 \in T$ **do**
3: **for** each type $t2 \in T$ **do**
4: **for** $i = 1$ to $d$ **do**
5: $P =$ a set of patterns which have one $t1$ and one $t2$ with the distance $= i$
6: $sum = 0$
7: **for** each pattern $p \in P$ **do**
8: lithography simulation of $p$ after OPC
9: **for** each EPE hot spot $h \in p$ and $\geq$ noise **do**
10: sum+ $=$ EPE of $h$
11: **end for**
12: **end for**
13: WGT_TABLE $(t1, t2, i) = (sum/|P|)$
14: **end for**
15: **end for**
16: **end for**
17: **return** WGT_TABLE

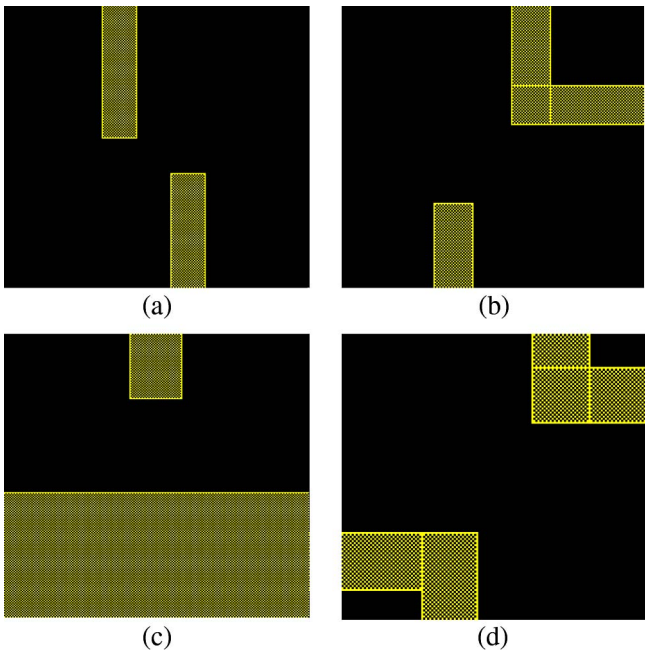


Fig. 5. Examples of various WGTs and their interactions. (a) Interaction between two line ends. (b) Interaction between a jog corner and a line end. (c) Interaction between a line end and a line edge of a fat wire or a metal pad. (d) Interaction between two jog corners.

For example, considering the technology in [1] and [12], we can regard the following shapes as WGTs:

1) **Via on M1-V1-M2:** via1, viar1 (rotated via1), via1_fat (2x fatter than via1), and via1r_fat (rotated via1_fat);
2) **Via on M2-V2:** via2, via2ts (stacked), via2_fat (ignored due to the same shape as via2ts on M2), and via2r_fat;
3) **Wire on M1 and M2:** line ends and line edge on fat wires;
4) **Jog on M1 and M2:** four jog corners for four possible turns, which are north–west, north–east, south–west, and south–east. In Fig. 5(d), north–west and south–east turns are shown;
5) **Others on M1 and M2:** metal pad.

Since a set of WGTs are highly fab/process dependent and can be different for each manufacturer and each technology generation, fast characterization is highly required. Let $N$ be the number of WGTs, $W$ be the size of the effective window of lithography, and $m$ be the minimum wire width. With pattern symmetry taken into account, the number of configurations for each pair of WGTs would be $(W/2m)$. Thus, the total number of cases is $(N(N-1)/2)\cdot(W/2m)$, which can be characterized in a few hours including OPC, according to our experience. Therefore, the characterization update can be done in a short time, and each characterization triple (the line 13 of Algorithm 1) needs only 4 B and $O(1)$ access time by table lookup. Consequently, with statistical WGT characterization, we can see advantages over pattern characterization in terms of run time and space. Moreover, as any polygon can be decomposed into grids geometrically, we can estimate printability *incrementally*, which is critical for a DR. Then, the question is about the fidelity of our metric, which will be shown in Section V-C.

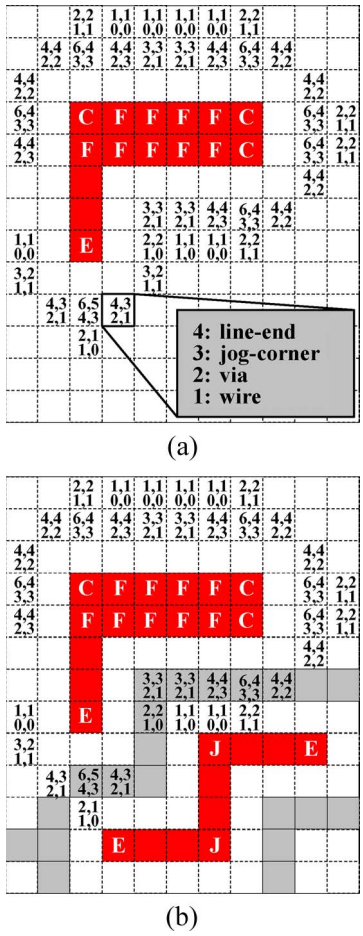


Fig. 6. Respectively assuming C, F, E, and J as blockage corner, fat wire edge, line end, and jog corner, respectively, WG_Shadowing examples are shown. Each grid has a cost array which contains the costs for jog corner, line end, via, and wire. (a) WG_Shadowing is performed along the contour of the blockage. Hence, grids within a certain distance get shadowed by a cost array. (b) WG_Shadowing needs to be performed along the routed wire. Thus, the costs in the arrays of the gray grids will be updated/increased.

### B. Compact Litho-Metric With OPC

The characterization from Algorithm 1 can be utilized to estimate printability during detailed routing. We propose the following litho-metric for a detailed routing grid $e$:

$$litho(e) = \begin{cases} e.cost[t], & \text{if WGT of } e = t \\ 0, & \text{otherwise} \end{cases} \quad (2)$$

where $e.cost[t]$ is a lithography cost computed by Algorithm 2. Fig. 6 shows an example of WG_Shadowing around a blockage and a net. For each WG, we will shadow neighboring grids within the effective window of lithography. While shadowing a grid, we prepare costs for all possible WGTs, so that the grid has a cost array as in line 5 in Algorithm 2. In Fig. 6(a), each grid has four costs, which will penalize any new polygon passing it by the corresponding cost. Later, if a wire is embedded in one of these shadowed grids, it gets a lithography penalty based on the WGT (e.g., whether a via is dropped, a line is ended, and so on) by (2). After the wire is embedded, we will perform WG_Shadowing for grids around the wire, as in Fig. 6(b).

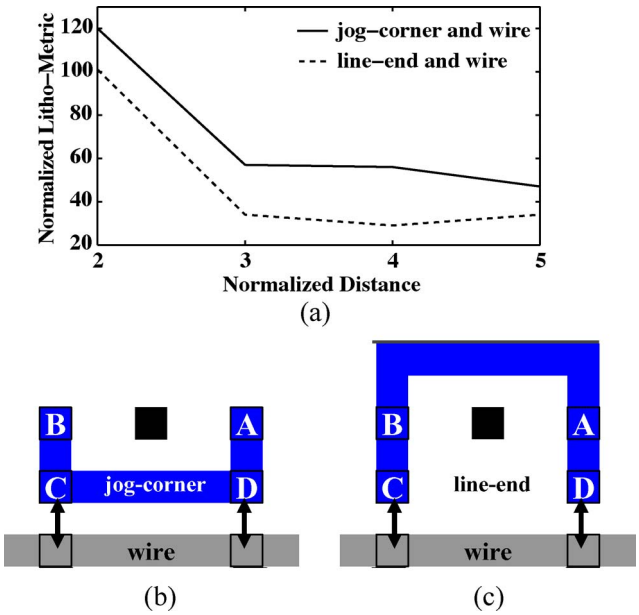


Fig. 7. A, B, C, and D are connected based on wire length in (b), but litho-metric in (c). (a) According to our WGT characterization, line end is cheaper than jog corner when faced with wire. (b) Wire length driven. (c) Litho-metric aware.

**Algorithm 2** WG_Shadowing
**Require:** A Table WGT_TABLE, a grid $e$, a set of WGTs $T$, a max distance $d$
1: $G =$ a set of grids within $d$ from $e/\{e\}$
2: $t =$ a WGT embedded at $e$
3: **for** each grid $g \in G$ **do**
4: **for** each type $t^* \in T$ **do**
5: $g.cost[t^*] +=$ WGT_TABLE($t, t^*$,dist from $g$ to $e$)
6: **end for**
7: **end for**

Such *what-if* costs in the array help find the minimum cost path in terms of wire length and litho cost [see (6)]. During graph search (typically, $A^*$ search or maze routing), we compute which WGT will be dropped at the currently visiting grid (by looking back at the previously visited grids and considering the propagation direction) and then increase the cost dynamically according to the *what-if* cost array. The same grid can be visited twice with different WGTs, and the less expensive path will be selected.

Unlike design rules, we can quantify the interaction between two WGTs in order to make beneficial tradeoffs among various routing patterns or design objectives. As in Fig. 7(a), line end is cheaper than jog corner when interacting with wire in our environment, although the litho-metrics of both decrease sharply with longer distance. Hence, our metric based on the characterization in Fig. 7(a) prefers the layout in Fig. 7(c) to that in Fig. 7(b) for better printability at a cost of wire length.

### C. High Fidelity of Our Litho-Metric

We evaluate the fidelity of our litho-metric by comparing with Calibre OPC/ORC (for detailed setup, see Section VII). Fig. 8 shows the high fidelity of our litho-metric, where $X$ and $Y$ axes are the normalized litho-metric and the normalized summation of EPEs, respectively. We collect the samples from industrial 65-m design layouts, while varying the sample size from $8 \times 8$ to $32 \times 32$ $\mu$m$^2$. When the sample area is $8 \times 8$ $\mu$m$^2$, as in Fig. 8(a) and (b), it does not correlate with the simulation result well enough to guide a DR. However, the larger the sample area is, the better it correlates, as shown in Fig. 8(c)–(f). When the sample area is $32 \times 32$ $\mu$m$^2$, it correlates more than 95% for both M1 and M2, where most litho hot spots occur. The reason for higher fidelity for larger sample is because we take the average of EPE for each distance during WGT characterization, as line 13 of Algorithm 1. With smaller sample area where we may get some extreme cases, the prediction can deviate from the real trend. Statistically, however, with larger sample area where we can get enough cases to capture the statistically real trend, the prediction gets more accurate.

Low correlation in small area is not a problem for us, as the goal of our metric is to capture the overall printability for the entire chip. It is obvious that our metric cannot capture the fine scale lithography effect, but it should be enough to guide optimization globally. If we guide a DR using our metric, we can obtain a globally litho-friendly layout, which is exactly our objective in design-time printability optimization.

## VI. ELIAD Algorithm

In this section, we propose our algorithm for an ELIAD router. Our router is guided by the metric in Section V, based on a Lagrangian relaxation technique which will be discussed in Section VI-A. The overall algorithm is proposed in Section VI-B.

### A. Problem Formulation

We can mathematically formulate a lithography aware detailed routing problem as follows:

$$\begin{aligned} \min_P: \quad & \sum_{e \in P} 1 \\ \text{s.t}: \quad & litho(e) \le L \qquad \forall e \in P \end{aligned} \tag{3}$$

where the objective is to minimize wire length and the constraint is to keep $litho(e)$ from (2) less than a given threshold $L$. Note that, if $L$ is too small, it can make (3) infeasible, but too large $L$ will degrade the solution quality. If we treat the cost array in each grid as a weight vector, optimally solving (3) is equivalent to finding MCSP [8], which is proven to be NP-hard [31]. Therefore, we use Lagrangian relaxation by introducing Lagrangian multiplier $\lambda_e$ for each grid in the design. Then, by relaxing constraints, we can show the following [15], [27], [31]:

$$\begin{aligned} S^* &= \min_P \left\{ \sum_{e \in P} 1 : litho(e) \le L \right\} \\ &\ge \min_P \left\{ \sum_{e \in P} 1 + \lambda_e (litho(e) - L) : litho(e) \le L, \lambda_e \ge 0 \right\} \\ &\ge \min_P \left\{ \sum_{e \in P} 1 + \lambda_e \left( litho(e) - L \right) : \lambda_e \ge 0 \right\} \end{aligned} \tag{4}$$

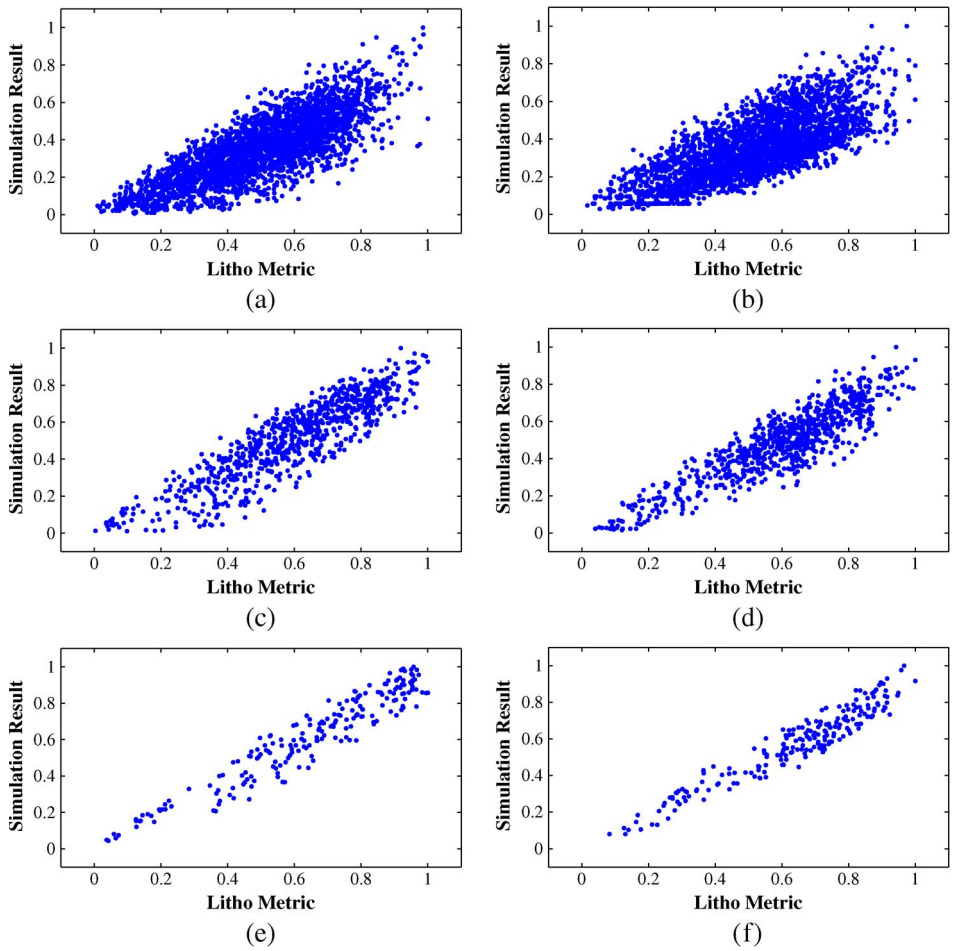


Fig. 8. Our litho-metric shows higher fidelity to post-OPC printability in larger scale. (a) $R = 0.81$ and $8 \times 8$ $\mu$m$^2$ in M1. (b) $R = 0.75$ and $8 \times 8$ $\mu$m$^2$ in M2. (c) $R = 0.89$ and $16 \times 16$ $\mu$m$^2$ in M1. (d) $R = 0.90$ and $16 \times 16$ $\mu$m$^2$ in M2. (e) $R = 0.96$ and $32 \times 32$ $\mu$m$^2$ in M1. (f) $R = 0.95$ and $32 \times 32$ $\mu$m$^2$ in M2.

$$\geq \max_{\lambda} \min_{P} \left\{ \sum_{e \in P} 1 + \lambda_e \left( litho(e) - L \right) : \lambda_e \geq 0 \right\}. \tag{5}$$

The implication from (4) is that the maximum lower bound of the optimal solution for (3) can be obtained by solving the following Lagrangian subproblem:

$$\begin{aligned} \max_{\lambda} \min_{P} : \quad & \sum_{e \in P} 1 + \lambda_e \left( litho(e) - L \right) \\ \text{s.t.} : \quad & \lambda_e \geq 0 \qquad \forall e \in P \end{aligned} \tag{6}$$

which can be solved by repeatedly finding the min-cost path for each net after assigning $1 + \lambda_e litho(e)$ as the routing cost to a grid $e$. Moreover, the optimal solution of (6) is the optimal solution of (3) under some conditions. See [31] for details. Since (6) is a convex programming and $litho(e)$ is not differentiable everywhere, we can use a subgradient method to solve (6) in ELIAD as in Section VI-B.

### B. Algorithm

As discussed in Section VI-A, we can implement ELIAD by solving (6) as in Algorithm 3. In lines 1–6, we perform WG_Shadowing for the existing blockages. In detailed routing, power/ground network, clock network, pins/connections from standard cells, and timing critical nets are already embedded, forming routing blockages. Hence, we should detect the contour of each blockage and perform WG_Shadowing around it. Since a blockage can be in a complicated shape, we use Moore-neighbor tracing algorithm [13] for contour detection in our implementation. In lines 7–20, we use subgradient method, where the min-cost path minimizing the objective of (6) for each net is searched, and update $\theta$ as follows:

$$\theta = \begin{cases} k^{-\alpha}, & \text{if } litho(e) > L \\ -k^{-\alpha}, & \text{otherwise} \end{cases} \tag{7}$$

where $k$ is the iteration index, and $\alpha (< 1)$ is a parameter that provides a tradeoff between solution quality and convergence rate. For $L$, we use the minimum cost in WGT_TABLE (the smallest nonzero $litho(e)$) to mainly purse a high quality solution. Since a new route is not only influenced by neighbors but also affects them, we need multiple iterations to converge. Subgradient method to solve MCSP is already used in [15], [27], and [31], but our algorithm has two key improvements in terms of memory and convergence. First, in [15] and [31], each detailed routing grid needs to have a cost array which should be as big as the number of nets in the design. As the number of nets is over thousands for even small application-specified integrated circuit (ASIC), it may result in unacceptable memory overhead. However, ours requires a cost array which is just

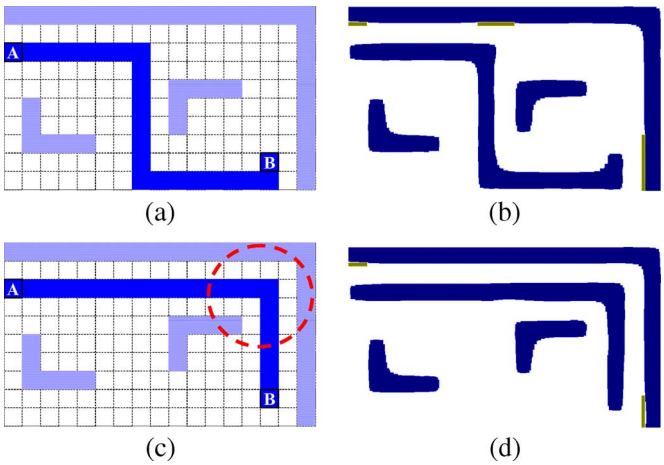


Fig. 9. Simple rule-based routing can be inaccurate, while not only producing more hot spots but also increasing wire length. (a) Twenty-one-grid long path from $A$ to $B$ is with extra spacing rule for line-end design. (b) Calibre OPC/ORC result of (a) shows six hot spots with $DOF = 0.1$ $\mu$m. (c) Nineteen-grid long path from $A$ to $B$ is found by our litho-metric. (d) Calibre OPC/ORC result of (c) shows two hot spots with $DOF = 0.1$ $\mu$m.

as big as the number of WGTs (in general, around ten, as in Section V-A). Second, different from [15] and [31], we achieve faster convergence by starting with small nonzero Lagrangian multipliers ($\lambda_e$) and performing WG_Shadowing after each net is routed. Since most modern designs may have litho hot posts very likely, it is better to start with nonzero $\lambda_e$. We initially set $\lambda_e$ such that a wire cost [which is one as in (3)] can be identical to the minimum cost in WGT_TABLE. Hence, even the first iteration will be lithography aware for faster convergence.

**Algorithm 3** ELIAD

**Require:** A set of blockages $K$, a set of nets $N$, a table WGT_TABLE, a max distance $d$

```
for each blockage k ∈ K do
    G =a set of grids from contour of k
    for each grid g ∈ G do
        WG_Shadowing(WGT_TABLE, g, d)
    end for
end for
λ_e = ε > 0, ∀e in design
repeat
    P ⇐ ∅
    for each net n ∈ N do
        M =a set of grids on min-cost path of n by Eq. (6)
        for each grid m ∈ M do
            WG_Shadowing(WGT_TABLE, m, d)
        end for
        P = P ⋃ M
    end for
    for each grid e ∈ P do
        λ_e = max(0, λ_e + θ · litho(e))
    end for
until max iteration
```

Our approach achieves *true* lithography awareness in a sense that a DR can produce a globally litho-friendly layout while considering OPC. Fig. 9 shows the layouts which differentiate ours from the prior works. While existing works (which either use manufacturability rules or ignore OPC) falsely detect litho hot spots, ours can nail down a real hot spot to reduce the run time and quality overhead.

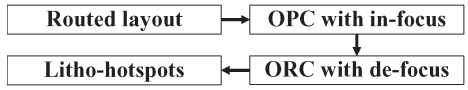


Fig. 10. Industrial Calibre OPC/ORC flow.

## VII. Experimental Results

We implemented ELIAD in C++ and tested with two industrial 65-nm ASIC designs on Intel Xeon 2.4-GHz Linux machine with 4G RAM. We used Calibre OPC/ORC from Mentor Graphics for model-based OPC and ORC. Our optical parameters were wavelength $(\lambda) = 193$ nm, $NA = 0.85$, and annular illumination $\sigma = 0.92/0.72$. The thicknesses of photoresist and bottom antireflective coating were 0.165 and 0.038 $\mu$m, respectively. As in industrial practice, we also had a tolerance to the EPE of line ends and convex and concave corners with 0.1 and 0.09 $\mu$m, respectively. Fig. 10 shows our overall flow for Calibre OPC/ORC. Following industrial practice, our characterization in Section V was done under the in-focus condition after full OPC, but a defocus condition with $DOF = 0.1$ $\mu$m was assumed during ORC.

Table I clearly emphasizes the necessity of the post-OPC printability metric by comparing pre- and post-OPC EPEs of the same location in a 65-nm ASIC design. In detail, based on the ORC of the un-OPCed design, we scan each detailed routing grid in the design and then find 544 thousand points with nonzero EPEs. As in the first row of Table I, the distribution of EPEs from un-OPCed design ranges from 1 to 32 nm. Meanwhile, we perform ORC again on the same but OPCed design to get new EPEs for the 544 thousand points, which ranges from 1 to 21 nm, as in the first column. Then, we compute the distribution of corresponding post-OPC EPE values for each pre-OPC EPE, as in Table I. For example, a point with 32-nm EPE before OPC may have 3-nm EPE after OPC with 88.4% probability. We also mark the largest probability for each pre-OPC EPE in bold to show the trend. As explained in Section IV, there is little correlation $(R = -0.36)$ between pre- and post-OPC EPEs due to highly advanced OPC algorithms.

For thorough comparison, we prepared a conventional grid-based **DR**, as well as a lithography-aware **RR** like RADAR [21]. Instead of lithography simulation without OPC [21], we applied OPC in RR as well for more accurate hot spot detection. Therefore, we had four different routers: **DR**, **DR** + **RR**, **ELIAD**, and **ELIAD** + **RR**. Fig. 11 shows these routing algorithms. We used $A^*$ search to find min-cost path in all the routers, and our $A^*$ search implementation guarantees the optimality by using an admissible and monotonic heuristic cost function.

Table II comprehensively compares the results from all the routers. It shows that ELIAD significantly improves the overall EPE for both designs. In terms of M1 hot spot (with 15-nm EPE tolerance), ELIAD has 75% less than DR, 66% less than DR + RR for ckt1, and 84% less than DR and DR + RR

TABLE I
PRE- AND POST-OPC EPE MAPPING BASED ON 544 K SAMPLING POINTS SHOWS THAT THEY ARE HIGHLY UNCORRELATED ($R = -0.36$)

| Post-OPC EPE ($nm$) \ Pre-OPC EPE ($nm$) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 12.0 | 7.3 | 8.2 | 2.6 | 0.9 | 0.8 | 0.4 | 1.6 | 3.9 | 3.0 | 2.2 | 4.3 | 7.7 | 9.2 | 1.8 | 3.5 | 3.7 | 1.9 | 1.8 | 2.2 | 3.1 | 5.2 | 18.0 | 10.7 | 7.9 | 16.7 | 10.1 | 8.3 | 3.2 | 8.3 | 13.9 | 0 |
| 2 | **55.6** | **64.3** | **45.4** | 26.8 | 5.9 | 0.8 | 1.8 | 3.6 | 4.6 | 5.4 | 21.7 | 17.4 | 19.3 | **46.8** | **38.9** | *62.5* | **67.0** | **72.2** | **63.1** | **57.6** | **59.7** | **50.3** | **41.2** | **55.3** | **50.7** | 5 0 | 28.5 | **63.0** | **57.4** | **63.6** | 43.0 | 11.6 |
| 3 | 11.3 | 17.0 | 29.6 | **38.4** | 10.4 | 3.3 | 1.3 | 0.1 | 0.7 | 0.7 | 0.3 | 5.6 | 1.3 | 8.7 | 5.2 | 13.6 | 15.6 | 20.4 | 29.7 | 38.6 | 35.7 | 33.2 | 36.0 | 31.7 | 25.9 | **30.5** | **41.9** | 23.9 | 39.1 | 28.1 | **43.1** | **88.4** |
| 4 | 6.8 | 7.7 | 15.7 | 15.9 | **39.9** | 10.1 | 2.7 | 0.4 | 0 | 0.1 | 0.4 | 0.1 | 0 | 0 | 0.1 | 0.1 | 0.9 | 1.8 | 1.1 | 0.5 | 0.6 | 0.6 | 0.9 | 1.4 | 0.3 | 0.2 | 0.1 | 2.8 | 0.1 | 0 | 0 | 0 |
| 5 | 1.8 | 2.0 | 1.1 | 9.3 | 29.0 | **38.3** | 3.4 | 2.1 | 0.2 | 0 | 0 | 0.2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.1 | 0.3 | 0.1 | 0 | 0 | 0.1 | 0.1 | 1.4 | 0.2 | 0 | 0 | 0 |
| 6 | 0.3 | 0.2 | 0.1 | 6.9 | 8.7 | 31.2 | 31.7 | 13.1 | 6.4 | 0.2 | 0 | 0 | 0 | 1.9 | 0 | 0 | 0.1 | 0.1 | 0 | 0 | 0 | 0.1 | 0.1 | 0 | 0 | 0 | 0 | 0.1 | 0 | 0 | 0 | 0 |
| 7 | 1 0 | 1.5 | 0 | 0.2 | 5.1 | 9.0 | **40.6** | **33.4** | 13.5 | 4.1 | 0.4 | 0.1 | 0 | 2.7 | 0.1 | 0.1 | 0 | 0 | 0 | 0.2 | 0.6 | 0 | 0 | 0 | 0 | 0 | 0 | 0.2 | 0 | 0 | 0 | 0 |
| 8 | 1.7 | 0 | 0 | 0 | 0 | 6.1 | 8.7 | 31.8 | 23.8 | 12.3 | 2.0 | 1.3 | 0.3 | 0.1 | 0.1 | 2.7 | 0.1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9 | 0.4 | 0 | 0 | 0 | 0 | 0.5 | 9.2 | 10.5 | **31.5** | 21.4 | 9.8 | 0.9 | 0.1 | 1.1 | 0.1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10 | 0 | 0 | 0 | 0 | 0 | 0 | 0.3 | 2.8 | 10.6 | **36.3** | 17.7 | 11.1 | 12.8 | 0.3 | 0.1 | 0.2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.5 | 2.9 | 11.0 | **29.7** | 12.3 | 19.8 | 3.2 | 0.2 | 0.7 | 0.2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 12 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1.7 | 3.6 | 14.7 | **38.7** | **21.7** | 5.9 | 1.2 | 1.2 | 0.2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1.9 | 1.0 | 7.8 | 13.1 | 11.9 | 6.9 | 2.3 | 5.2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.1 | 3.6 | 5.4 | 26.4 | 4.6 | 4.9 | 0.2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2.7 | 18.9 | 6.4 | 1.5 | 1.8 | 0.1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.1 | 0 | 2.0 | 0.3 | 0.7 | 1.9 | 0.1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 17 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.2 | 0.6 | 1.9 | 0.1 | 0 | 0.5 | 0.1 | 0.1 | 0.2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 18 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.2 | 0.4 | 0.7 | 0 | 0.1 | 0.5 | 0.4 | 1.0 | 0.2 | 0 | 0 | 0 | 0 | 0 | 0 |
| 19 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 9.7 | 1.4 | 0.3 | 13.5 | 0.2 | 0 | 0 | 0 | 0 | 0 | 0 |
| 20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1.6 | 0.1 | 0.5 | 2.1 | 3.3 | 0 | 0 | 0 | 0 | 0 |
| 21 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 16.0 | 0.2 | 0 | 0 | 0 | 0 |

The median mapping points are in a bold font.

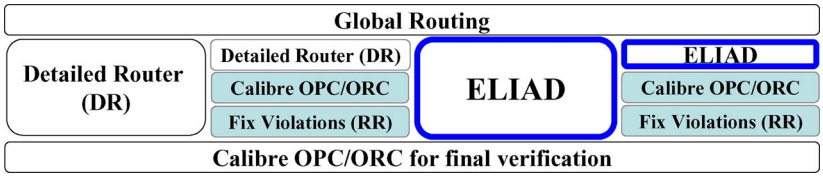


Fig. 11. Experimental flow with four different routing algorithms [15].

TABLE II
COMPARISON BETWEEN VARIOUS ROUTERS ON TWO INDUSTRIAL DESIGNS

| design | router | wirelen ($mm$) | runtime breakdown (sec) | | | EPE ($nm$) | | | | | | Ratio | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | M1 | | | M2 | | | | M1 | M2 |
| | | | router | OPC/ORC[a] | total | 5–10 | 10–15 | **15+** | 5–10 | 10–15 | **15+** | runtime | hotspot[b] | hotspot[b] |
| ckt1 59.5K $um^2$ 5.6K nets | DR | 6002.4 | 509.9 | n/a | 509.9 | 16572 | 5182 | **285** | 7468 | 4304 | **90** | 1 | 4.0 | 15.0 |
| | DR+RR [21] | 6008.0 | 835.3 | 7529.0 | 8364.3 | 13592 | 4549 | **226** | 4831 | 2176 | **82** | 16.4 | 3.1 | 13.7 |
| | ELIAD | 6003.5 | 798.6 | n/a | 798.6 | 1985 | 985 | **76** | 257 | 37 | **6** | 1.6 | 1.1 | 1 |
| | ELIAD+RR[a] | 6008.1 | 1194.5 | 7775.6 | 8969.1 | 1774 | 895 | **72** | 221 | 27 | **6** | 17.6 | 1 | 1 |
| ckt2 50.2K $um^2$ 7.9K nets | DR | 10168.5 | 353.8 | n/a | 353.6 | 17124 | 5834 | **424** | 4082 | 2062 | **54** | 1 | 7.6 | 27.0 |
| | DR+RR [21] | 10175.1 | 606.4 | 6654.1 | 7260.5 | 14104 | 5127 | **394** | 2614 | 1385 | **49** | 20.5 | 7.0 | 24.5 |
| | ELIAD | 10169.6 | 491.9 | n/a | 491.9 | 1318 | 1209 | **69** | 354 | 22 | **2** | 1.4 | 1.2 | 1 |
| | ELIAD+RR | 10174.8 | 767.8 | 6688.4 | 7456.2 | 1179 | 1125 | **56** | 331 | 18 | **0** | 21.1 | 1 | - |

[a] The runtime ratio between OPC (8 iterations) and ORC is about 2.5 : 1 according to our experiments.
[b] EPE tolerance for litho-hotspot is $15nm$.

for ckt2. The reduction is even much more for M2 hot spot, at least 93% and 96% for ckt1 and ckt2, respectively. When ELIAD is combined with RR (ELIAD + RR), it can further improve printability (about 10%). This implies that ELIAD, which is a correct-by-construction approach, is highly superior to postoptimization (RR) approach but can be complementary with it (RR) by providing an excellent starting point. Regarding run time, while ELIAD is at most 60% slower than DR, RR involves huge overhead mainly from hot spot detection using expensive OPC/ORC. ELIAD is at least ten times faster than any approach with RR (DR + RR and ELIAD + RR). Finally, there is a negligible difference among routers in terms of wire length.

Table III further analyzes the performance of ELIAD by comparing EPE reduction with DR + RR in a partition-by-partition manner. As expected, ELIAD yields significantly better EPE reduction, but our point here is that ELIAD can improve EPE globally, while DR + RR cannot. When we compute the coefficient of variance (cov) of hot spot reduction over 12 partitions (P1–P12) for ELIAD and DR + RR, ELIAD and DR + RR have 0.45 and 0.046, respectively. The implication of ten times smaller cov is that the performance of RR highly depends on the complexity of the initial routing and local congestion (e.g., hard to find a totally new routing path), as it cannot make radical change to improve printability. However, since ELIAD runs in a correct-by-construction way from the scratch, it can consistently improve printability all over the place. This situation can also be observed from the Fig. 6 in RADAR [21], where most of hot spot removals are from the outer regions rather than the core.

TABLE III
DETAILED EPE REDUCTION (IN PERCENT) OVER DR COMPARISON BETWEEN DR + RR AND ELIAD BY PARTITION

| router | DR+RR [21] | | | | | | | | ELIAD | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| design | ckt1 | | | | ckt2 | | | | ckt1 | | | | ckt2 | | | |
| layer | M1 | | M2 | | M1 | | M2 | | M1 | | M2 | | M1 | | M2 | |
| EPE ($nm$) | 5–10 | 10+ | 5–10 | 10+ | 5–10 | 10+ | 5–10 | 10+ | 5–10 | 10+ | 5–10 | 10+ | 5–10 | 10+ | 5–10 | 10+ |
| P1 | 31.4 | 30.5 | 13.5 | 49.3 | 14.5 | 14.4 | 36.1 | 36.6 | 82.1 | 73.2 | 91.7 | 98.9 | 92.9 | 77.9 | 90.4 | 100.0 |
| P2 | 21.9 | 13.1 | 33.0 | 55.7 | 12.1 | 7.3 | 37.3 | 37.0 | 82.8 | 69.8 | 90.3 | 98.8 | 91.7 | 74.5 | 90.6 | 99.1 |
| P3 | 22.8 | 17.6 | 24.5 | 46.7 | 16.7 | 11.1 | 40.2 | 31.4 | 83.5 | 74.4 | 92.4 | 98.8 | 90.0 | 79.0 | 94.0 | 99.2 |
| P4 | 11.6 | 1.9 | 35.8 | 40.3 | 32.9 | 34.3 | 44.0 | 53.8 | 92.7 | 77.7 | 84.7 | 97.0 | 90.5 | 91.4 | 84.0 | 100.0 |
| P5 | 9.6 | 8.5 | 37.8 | 41.5 | 18.6 | 17.8 | 16.7 | 16.0 | 95.4 | 88.6 | 99.1 | 98.8 | 90.4 | 76.9 | 92.3 | 99.5 |
| P6 | 18.4 | 10.5 | 46.9 | 55.5 | 19.4 | 19.6 | 37.2 | 39.2 | 91.9 | 86.5 | 99.9 | 100.0 | 88.6 | 73.5 | 91.4 | 99.5 |
| P7 | 12.7 | 20.1 | 40.8 | 51.1 | 14.4 | 22.4 | 41.3 | 41.3 | 88.2 | 85.1 | 99.9 | 98.6 | 91.8 | 81.6 | 89.0 | 97.1 |
| P8 | 9.4 | 0.0 | 10.3 | 22.4 | 8.2 | 21.7 | 37.8 | 50.0 | 85.9 | 91.1 | 99.1 | 100.0 | 95.9 | 91.7 | 97.3 | 95.5 |
| P9 | 9.1 | 19.2 | 43.6 | 51.8 | 19.8 | 20.5 | 37.9 | 38.0 | 93.1 | 87.2 | 99.5 | 99.1 | 94.4 | 86.5 | 90.8 | 99.5 |
| P10 | 16.7 | 15.1 | 41.1 | 52.2 | 17.1 | 19.8 | 30.7 | 28.5 | 93.4 | 91.5 | 99.8 | 100.0 | 93.7 | 85.4 | 92.4 | 98.2 |
| P11 | 16.3 | 17.7 | 49.5 | 59.0 | 23.0 | 24.3 | 46.4 | 38.6 | 83.5 | 84.7 | 99.7 | 99.7 | 95.7 | 87.4 | 91.2 | 99.1 |
| P12 | -8.3 | 10.0 | 34.9 | 58.5 | 43.4 | 48.1 | -14.8 | 23.1 | 94.8 | 95.0 | 100.0 | 100.0 | 94.6 | 86.4 | 88.9 | 100.0 |
| avg | 14.3 | 13.7 | 34.3 | 48.7 | 20.0 | 21.8 | 32.6 | 36.1 | 89.0 | 83.7 | 96.3 | 99.2 | 92.5 | 82.7 | 91.0 | 98.9 |
| std | 9.7 | 8.3 | 12.4 | 10.2 | 9,6 | 10.7 | 16.7 | 10.5 | 5.1 | 8.1 | 5.2 | 0.9 | 2.4 | 6.3 | 3.2 | 1.4 |
| cov ($\frac{std}{avg}$) | 0.68 | 0.61 | 0.36 | 0.21 | 0.48 | 0.49 | 0.51 | 0.29 | 0.06 | 0.10 | 0.05 | 0.01 | 0.03 | 0.08 | 0.03 | 0.01 |

## VIII. CONCLUSION

Manufacturability optimization during design stage receives larger attention than any time before due to aggressive technology scaling and delayed next-generation lithography systems. In this paper, we present ELIAD, which is a lithography aware detailed router in a correct-by-construction approach based on a fast yet high fidelity litho-metric with OPC consideration. Experimental results show that ELIAD is significantly superior to an RR technique or a postprocessing strategy, only at small run time overhead.

## REFERENCES


[1] S. N. Adya, S. Chaturvedi, J. A. Roy, D. Papa, and I. L. Markov, "Unification of partitioning, floorplanning and placement," in *Proc. Int. Conf. Comput. Aided Des.*, Nov. 2004, pp. 550–557.

[2] M. Born and E. Wolf, *Principles of Optics: Electromagnetic Theory of Propagation, Interference and Diffraction of Light*, 7th ed. Cambridge, U.K.: Cambridge Univ. Press, 1999.

[3] H.-Y. Chen, M.-F. Chiang, Y.-W. Chang, L. Chen, and B. Han, "Novel full-chip gridless routing considering double-via insertion," in *Proc. Des. Autom. Conf.*, Jul. 2006, pp. 755–760.

[4] T.-C. Chen and Y.-W. Chang, "Multilevel full-chip gridless routing with applications to optical-proximity correction," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 26, no. 6, pp. 1041–1053, Jun. 2007.

[5] M. Cho, H. Xiang, R. Puri, and D. Z. Pan, "Wire density driven global routing for CMP variation and timing," in *Proc. Int. Conf. Comput. Aided Des.*, Nov. 2006, pp. 487–492.

[6] M. Cho, H. Xiang, R. Puri, and D. Z. Pan, "TROY: Track router with yield-driven wire planning," in *Proc. Des. Autom. Conf.*, Jun. 2007, pp. 55–58.

[7] N. B. Cobb, "Fast optical and process proximity correction algorithms for integrated circuit manufacturing," Ph.D. dissertation, Univ. California, Berkeley, CA, 1998.

[8] J. Dong, J. Zhang, and Z. Chen, *Neural Network Based Algorithm for Multi-Constrained Shortest Path Problem*. Berlin, Germany: Springer-Verlag, 2007.

[9] T. E. Gbondo-Tugbawa, "Chip-scale modeling of pattern dependencies in copper chemical mechanical polishing process," Ph.D. dissertation, MIT, Cambridge, MA, 2002.

[10] P. Gupta, A. B. Kahng, and C.-H. Park, "Detailed placement for improved depth of focus and CD control," in *Proc. Asia South Pacific Des. Autom. Conf.*, Jan. 2005, pp. 343–348.

[11] L. He, A. B. Kahng, K. Tam, and J. Xiong, "Design of integrated-circuit interconnects with accurate modeling of CMP," *Proc. SPIE*, vol. 5756, pp. 109–119, Mar. 2005.

[12] [Online]. Available: http://vlsicad.eecs.umich.edu/BK/ICCAD04bench/

[13] [Online]. Available: http://www.cs.mcgill.ca/~aghnei/mmain.html

[14] S. Hu and J. Hu, "Pattern sensitive placement for manufacturability," in *Proc. Int. Symp. Phys. Des.*, Mar. 2007, pp. 27–34.

[15] L. Huang and D. F. Wong, "Optical proximity correction (OPC)-friendly maze routing," in *Proc. Des. Autom. Conf.*, Jun. 2004, pp. 186–191.

[16] A. B. Kahng, C.-H. Park, and X. Xu, "Fast dual-graph based hot-spot detection," in *Proc. BACUS Symp. Photomask Technol. Manage.*, 2006, p. 628 104.

[17] T. Kong, H. Leung, V. Raghavan, A. K. Wong, and S. Xu, "Model-assisted routing for improved lithography robustness," *Proc. SPIE*, vol. 6521, p. 652 10D, 2007.

[18] S.-Y. Kuo, "YOR: A yield-optimizing routing algorithm by minimizing critical areas and vias," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 12, no. 9, pp. 1303–1311, Sep. 1993.

[19] K.-Y. Lee and T.-C. Wang, "Post-routing redundant via insertion for yield/reliability improvement," in *Proc. Asia South Pacific Des. Autom. Conf.*, Jan. 2006, pp. 303–308.

[20] L. W. Liebmann, "Layout impact of resolution enhancement techniques: Impediment or opportunity?" in *Proc. Int. Symp. Phys. Des.*, 2003, pp. 110–117.

[21] J. Mitra, P. Yu, and D. Z. Pan, "RADAR: RET-aware detailed routing using fast lithography simulations," in *Proc. Des. Autom. Conf.*, Jun. 2005, pp. 369–372.

[22] D. Muller, "Optimizing yield in global routing," in *Proc. Int. Conf. Comput. Aided Des.*, Nov. 2006, pp. 480–486.

[23] Y. Pati, A. Ghazanfarian, and R. Pease, "Exploiting structure in fast aerial image computation for integrated circuit patterns," *IEEE Trans. Semicond. Manuf.*, vol. 10, no. 1, pp. 62–74, Feb. 1997.

[24] C. Spence, "Full-chip lithography simulation and design analysis: How OPC is changing IC design," *Proc. SPIE*, vol. 5751, pp. 1–14, 2005.

[25] R. Tian, D. F. Wong, and R. Boone, "Model-based dummy feature placement for oxide chemical–mechanical polishing manufacturability," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 20, no. 7, pp. 902–910, Jul. 2001.

[26] Y.-R. Wu, M.-C. Tsai, and T.-C. Wang, "Maze routing with OPC consideration," in *Proc. Asia South Pacific Des. Autom. Conf.*, Jan. 2005, pp. 198–203.

[27] G. Xu, L. Huang, D. Z. Pan, and D. F. Wong, "Redundant-via enhanced maze routing for yield improvement," in *Proc. Asia South Pacific Des. Autom. Conf.*, Jan. 2005, pp. 1148–1151.

[28] J. Xu, S. Sinha, and C. C. Chiang, "Accurate detection for process-hotspots with vias and incomplete specification," in *Proc. Int. Conf. Comput. Aided Des.*, Nov. 2007, pp. 839–846.

[29] H. Yao, S. Sinha, C. Chiang, X. Hong, and Y. Cai, "Efficient process-hotspot detection using range pattern matching," in *Proc. Int. Conf. Comput. Aided Des.*, Nov. 2006, pp. 625–632.

[30] P. Yu, S. X. Shi, and D. Z. Pan, "Process variation aware OPC with variational lithography modeling," in *Proc. Des. Autom. Conf.*, Jul. 2006, pp. 785–790.

[31] H. Zhou and D. Wong, "Crosstalk-constrained maze routing based on Lagrangian relaxation," in *Proc. IEEE Int. Conf. Comput. Des.*, Nov. 1997, pp. 628–633.

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