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Wed, Oct. 15
4:30-5:30 PM
ACES 2.302



Technology Outlook and VLSI Trends

ABSTRACT

I will begin with a brief overview of the IBM Austin Research Lab and current activities underway. This will be followed by a discussion on technology trends we have observed as part of IBM Research's annual Global Technology Outlook (GTO). We will then focus on key VLSI trends, specifically on power. The ability to manage and lower power is key to the design of systems ranging from handheld devices through high performance compute servers. Increasingly, overall system performance is now constrained by power. Thus, we must address power at all levels of the system performance stack: from technology, circuits, and microarchitecture through the multiple software layers and development tools. In addition, power efficient design must take place at all stages of the development cycle. This has always been the case for battery powered devices; but, is now standard operating procedure in the design of high performance information processing systems.

BIOGRAPHY

Michael Rosenfield is currently Director of the Austin Research Lab focusing on high performance VLSI design and tools, system level power analysis, and new system architectures. His previous position was Senior Manager of VLSI Design and Architecture at IBM T.J. Watson Research Center in Yorktown Heights, NY where he and his team were involved in high performance microprocessor VLSI design for IBM Server Group and Microelectronics, tools, methodologies, and commonality as well as power-aware microarchitecture, circuits/technology co-design, performance analysis, exploratory microarchitectures, and advanced compiler design. Previously, he has held management positions at Research in parallel communication architecture and in advanced lithography. In 1993, he was the technical assistant to the Research VP of Systems, Technology, and Science. He has a Ph.D and M.S. from the University of California, Berkeley and a B.S. in Physics from the University of Vermont.