EE382V: System-on-a-Chip (SoC) Design

Lecture 2 – DRM Project Overview

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Lecture 2: Outline

- **Marketing Requirements Document (MRD)**
  - Market focus
  - Product description
  - Cost metrics
  - Product features
  - References
- **Project description**
  - Overview
  - Hardware and software development tasks
  - TLL5000 Prototyping board

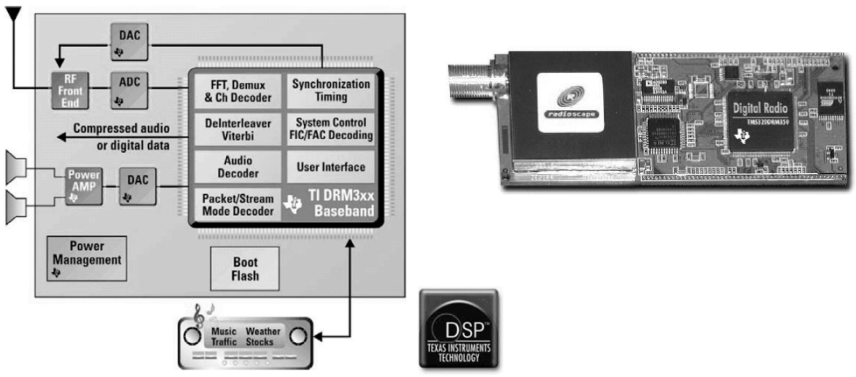
Market Focus

- **MP3 players that receive digital radio transmissions**
  - Estimated market size is approximately 5-7 million units per year
- **It is anticipated that the next generation cell phones may be configured to receive FM and DRM/DAB transmissions. If so…**
  - The potential market size is approximately 35 million units per year

➢ **What problem are we trying to solve?**
- There is a need to transmit and receive digital music and data using existing AM bands. Transmitters in these wavelengths are accessible world wide.
- Need to provide near-FM quality sound and the capacity to integrate data and text.

Competition

- **Texas Instruments TMS320DRM300/350**



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Product Description

- **DRM SoC to integrate into MP3 player or 4G cell phone.**
  - The hardware intellectual property will be delivered in a SystemC environment. This will include synthesizable RTL for all components which are not available in the standard library, such as accelerators, special I/O devices, etc.
- **DRM benefits**
  - Ability to receive digital music and data
    - Using existing long-, medium- and short-wave transmission systems
    - Providing near-FM quality sound and available to markets worldwide.
  - Small bandwidth of less than 20 kHz
    - Easy to handle with current generation of embedded computing devices.
  - Excellent audio quality
    - Significant improvement upon analog AM
    - Range of audio content, including multi-lingual speech and music
  - Capacity to integrate data and text
    - Additional content can be displayed to enhance the listening experience.
  - Use existing AM broadcast frequency bands
    - Designed to fit in with the existing AM broadcast band plan
    - Signals of 9 kHz or 10kHz bandwidth
    - Modes requiring as little as 4.5kHz or 5kHz bandwidth, plus modes that can take advantage of wider bandwidths, such as 18 or 20kHz.

Cost Metrics

- **Performance**
  - Utilize no more than 75 MHz of an ARM 926-EJS running at 256 MHz
- **Additional die size cost**
  - Accelerators < 0.5 mm^2
  - On board memory – TBD
- **Advanced system and power management**
  - Additional system power for accelerators < 8 mW

Product Features

- **Flexible and scalable platform based architecture**
  - Standard architecture for a wide range of devices supporting a wide range of services
  - Flexibility to dynamically re-program different digital radio standards tailored to particular scenarios
  - Portability to host third party designs on multiple independent platforms
  - ➢ Potential for significant life-cycle cost reduction
  - ➢ Over the air downloads of patches, new features & services
  - ➢ Significant improvement in flexibility, portability and interoperability between different users

Product Features (cont'd)

- **Technical features**
  - Frequency coverage: 0-32 MHz
  - Mode reception: USB, LSB, CW, AM, synchronous AM, NFM, DATA
  - Advanced IP3 greater than +35 dBm
  - Very high dynamic range
    - >100 dB in AM mode with 7 kHz filter
    - >105 dB in SSB mode with 2.2 kHz filter
    - >110 dB in CW mode with 500 Hz filter
  - Passband tuning: +/-5 kHz
  - Audio pitch tune in CW & DATA

DRM References

- **DRM consortium**
  - http://drm.org
- **Commercial DRM software radio (Frauenhofer)**
  - http://drmrx.org
- **Receiver hardware**
  - http://winradio.com

➢ **Open-source DRM software (DREAM)**
  - http://drm.sourceforge.net

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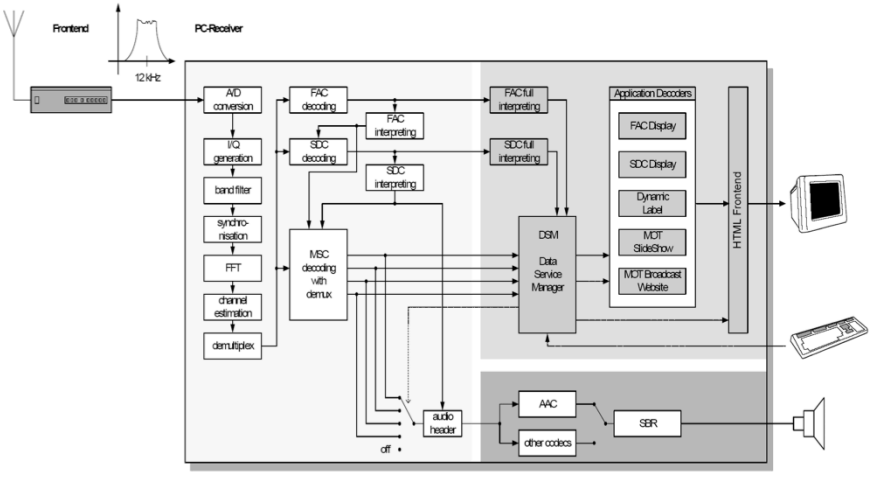
Project Description

- **HW/SW co-design of an embedded SoC**
  - Low-power DRM implementation
  - ARM-based target platform
    - ARM9 processor, memory components, I/O devices
    - Custom hardware accelerators
    - Interconnected via standard system bus
  - Virtual and physical prototyping
    - SystemC TLM-based virtual platform model (OVPsim ARM simulator)
    - ARM- and Xilinx FPGA-based prototyping board (TLL6219-TTL5000)
  - ➢ Lab and project teams

Project Objectives and Activities

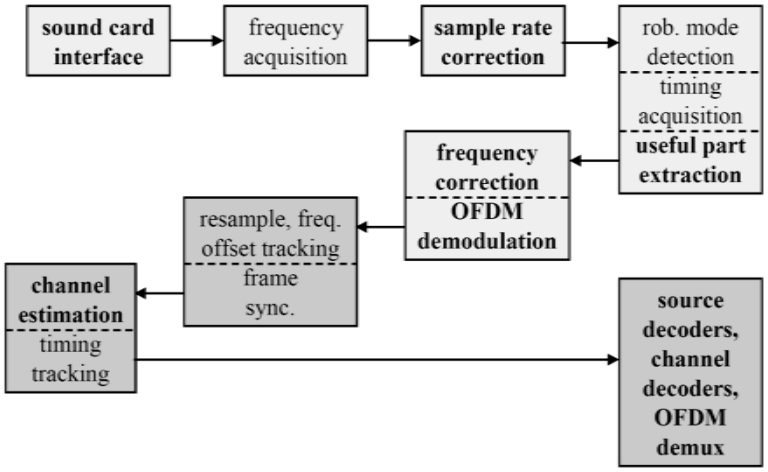
- **Project objective:**
  - Implement the DRM C++ code on a ARM based platform while meeting the performance, area and power metrics.
- **Project activities:**
  - Profile the DRM C++ software implementation to determine performance bottlenecks
  - Optimize the DRM C++ software for fixed point operation
  - Partition the software into components which will run on the ARM processor and on the hardware accelerators
  - Synthesize time-critical functions into Verilog for gate level implementation
  - Co-simulate and prototype the HW/SW implementation
  - Estimate timing, area and power metrics and validate against product requirements

PC-Based DRM System Architecture

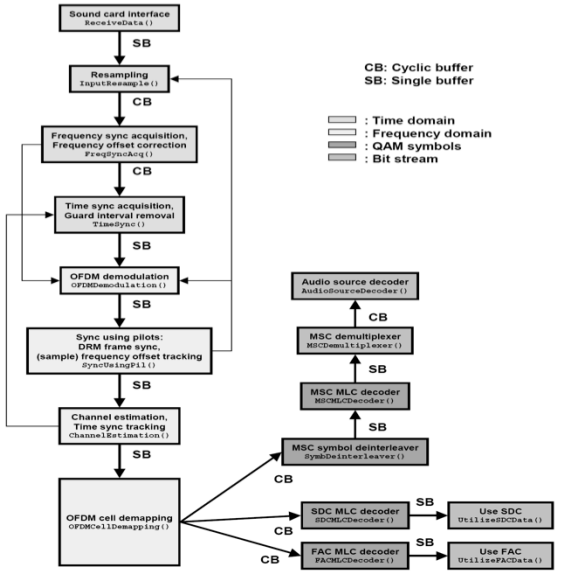


- **DRM reference code is designed to run on a desktop computer**

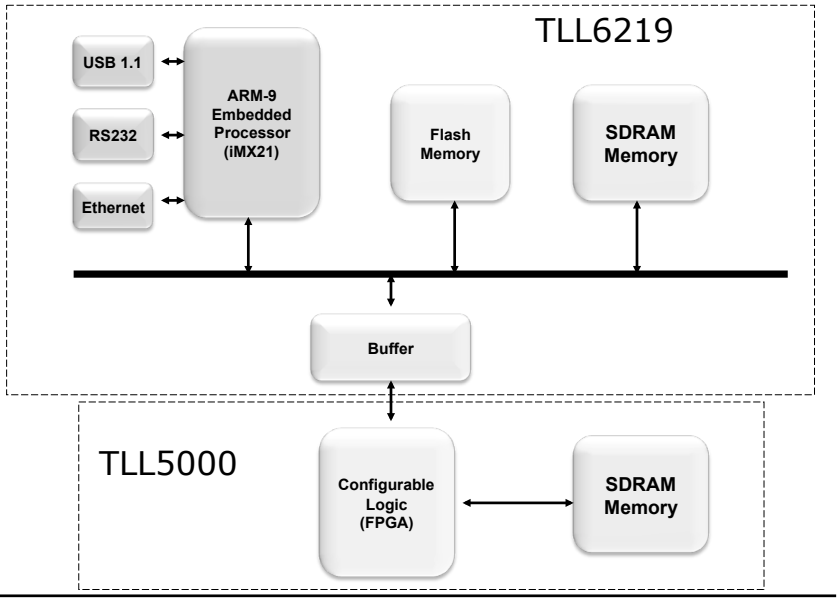
DRM Software Overview



DRM Software Architecture



High-Level Hardware Architecture



Development Tasks

- **Hardware development on FPGA**
  - Hardware accelerators (using synthesized code)
  - Interface to ARM board and on-chip bus
  - Interrupt logic
  - Clocking & reset
  - Optional memory controller (for external SDRAM)
  - Diagnostics
- **ARM software development**
  - Compile and profile DRM on ARM simulator
  - Convert floating-point to fixed-point code and check SNR
  - Compile and profile fixed-point DRM on ARM board
  - Develop hardware abstraction layer (HAL) and I/O handler
  - Develop interrupt handler

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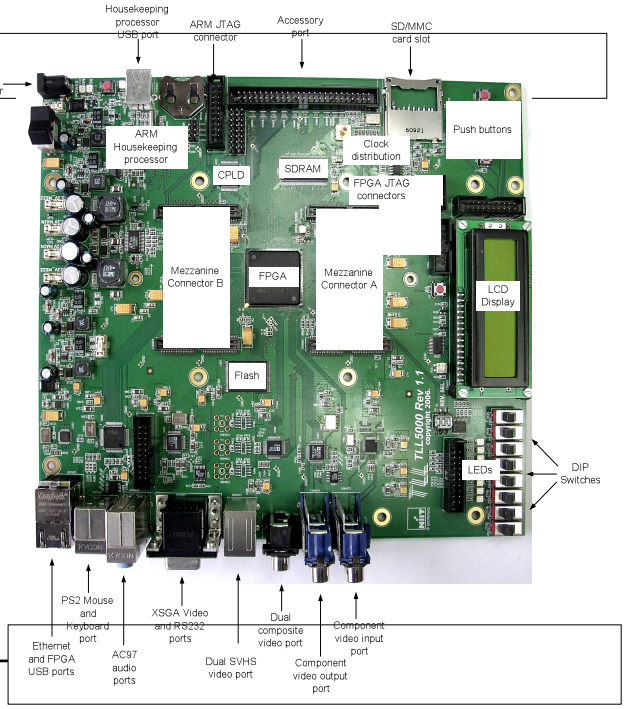
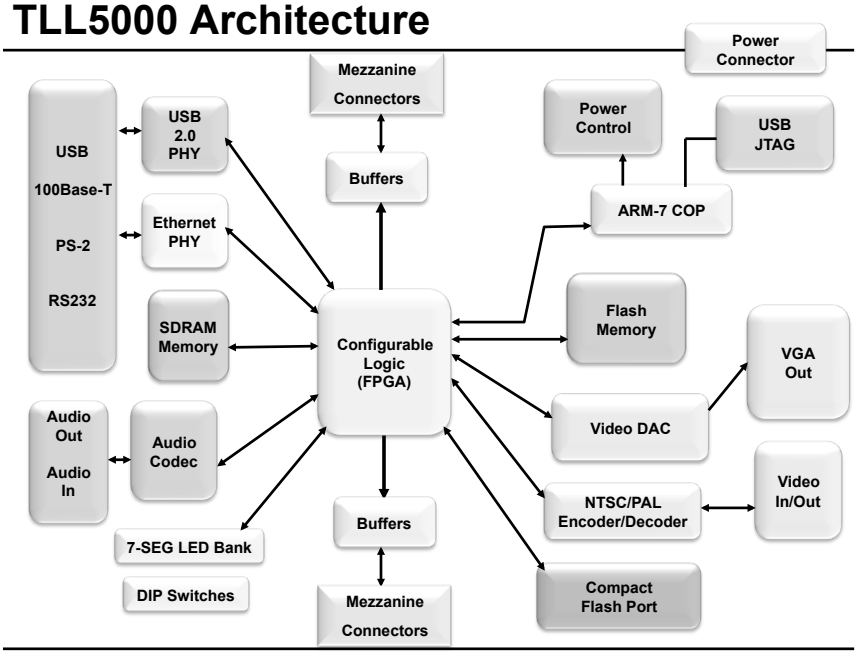
TLL5000

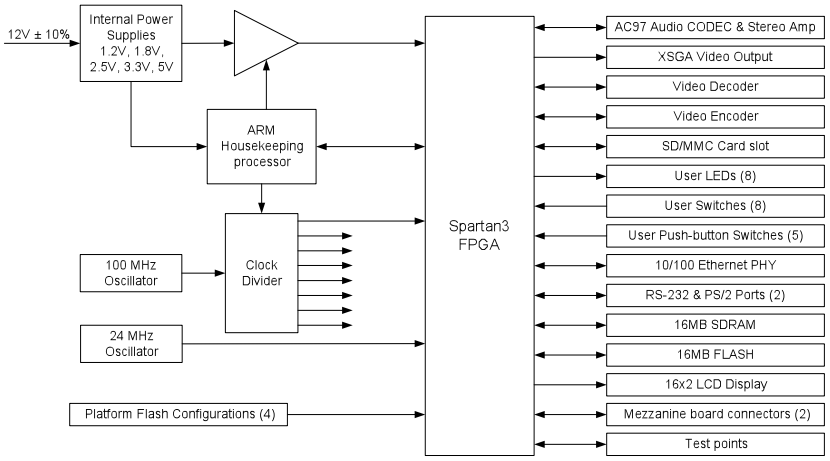
- **Prototyping platform**
  - Base board



TLL5000 Architecture



TLL5000 Block Diagram

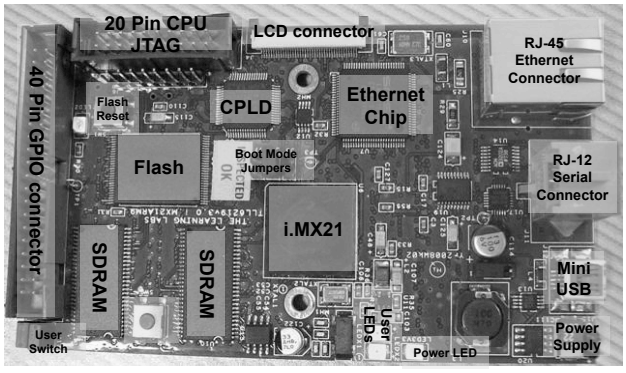


Xilinx Spartan 3 FPGA

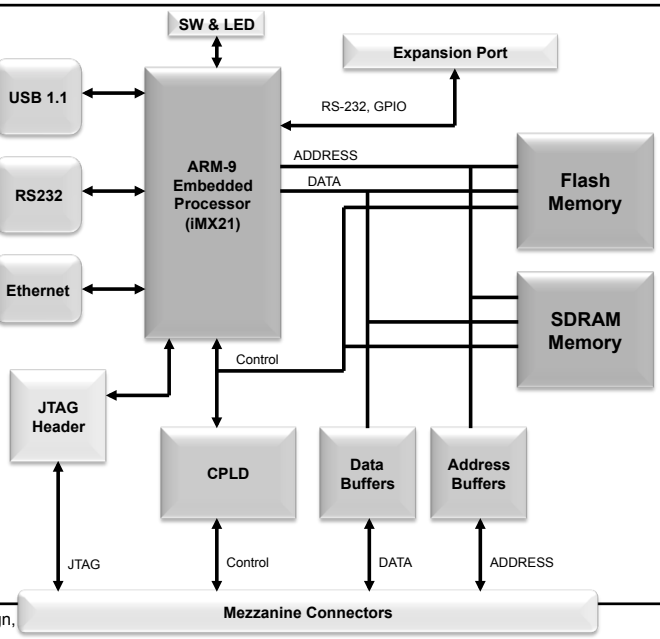
Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM Bits	Block RAM Bits	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XC3S50	50K	1,728	16	12	192	768	12K	72K	4	2	124	56
XC3S200	200K	4,320	24	20	480	1,920	30K	216K	12	4	173	76
XC3S400	400K	8,064	32	28	896	3,584	56K	288K	16	4	264	116
XC3S1000	1000K	17,280	48	40	1,920	7,680	120K	432K	24	4	391	175
XC3S1500	1500K	29,952	64	52	3,328	13,312	208K	576K	32	4	487	221
XC3S2000	2000K	46,080	80	64	5,120	20,480	320K	720K	40	4	565	270
XC3S4000	4000K	62,208	96	72	6,912	27,648	432K	1,728K	96	4	712	312
XC3S5000	5000K	74,880	104	80	8,320	33,280	520K	1,872K	104	4	784	344

Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	62	52	0	2	6	2
	1	61	51	0	2	6	2
Right	2	60	52	0	2	6	0
	3	60	52	0	2	6	0
Bottom	4	63	47	6	2	6	2
	5	61	45	6	2	6	2
Left	6	60	52	0	2	6	0
	7	60	52	0	2	6	0

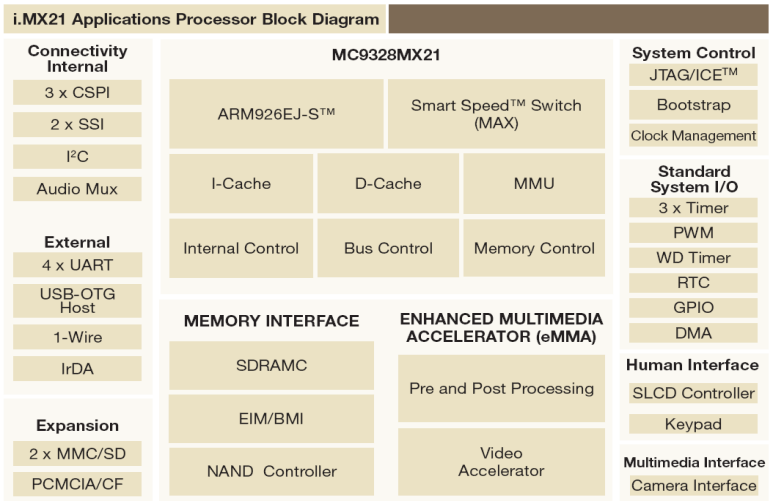
TLL6219 ARM Processor Board



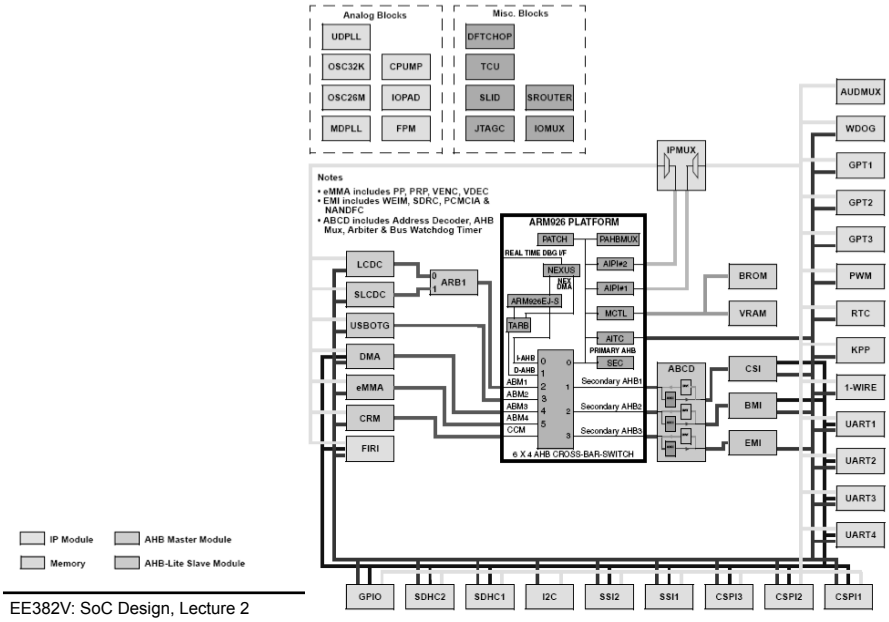
TLL6219 Block Diagram



i.MX21 Features



i.MX21 Block Diagram



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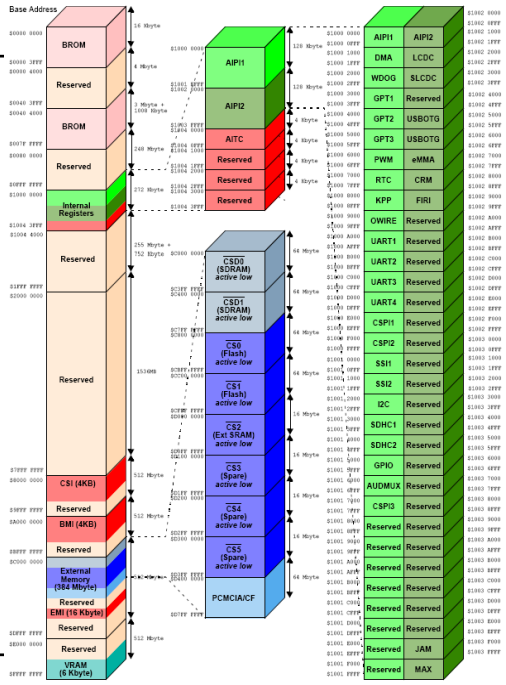
i.MX21 Memory Map

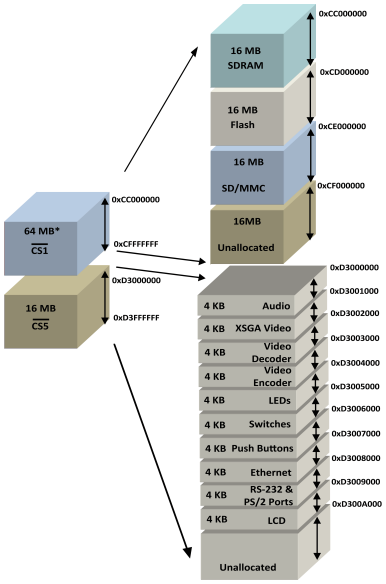
There are eight 512MB partitions

Address	Size	Usage
0x00000000	512 Mbyte	ROM, Primary AHB Slaves, and Peripherals
0x20000000	512 Mbyte	Reserved
0x40000000	512 Mbyte	Reserved
0x60000000	512 Mbyte	Reserved
0x80000000	512 Mbyte	Secondary AHB Slave Port 1
0xA0000000	512 Mbyte	Secondary AHB Slave Port 2
0xC0000000	512 Mbyte	Secondary AHB Slave Port 3
0xE0000000	512 Mbyte	Primary AHB (RAM)

Memory Map (1)



Memory Map (2)

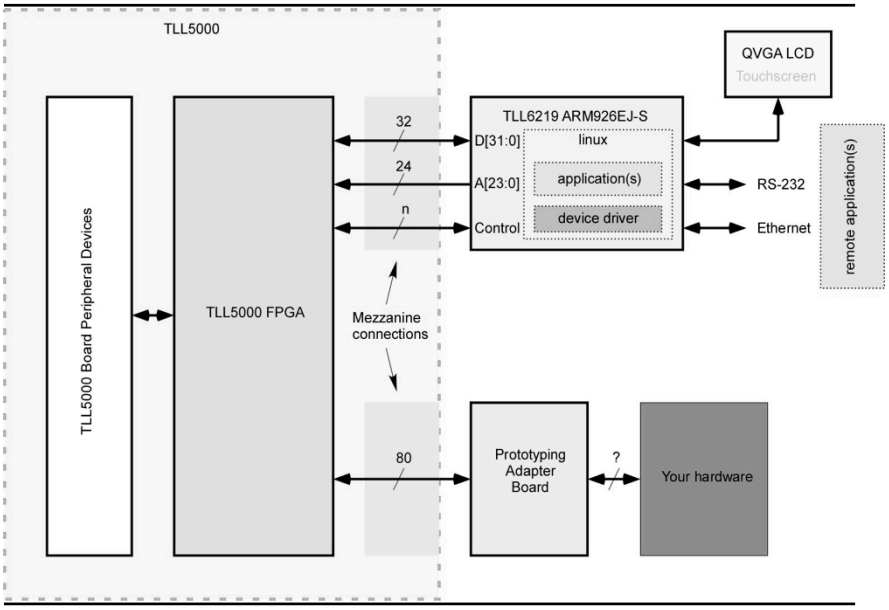


TLL6219 ARM926EJ-S Board

- **External interfaces**
  - RS-232 serial port
  - Ethernet
  - USB-OTG (Linux host driver for flash disk)
  - Graphic LCD panel
- **TLL5000 Interface**
  - External memory interface
    - /CS1, /CS5 memory regions
    - D[31:0], A[23:0], control signals (thru CPLD)
  - Connections to TLL6219 CPLD

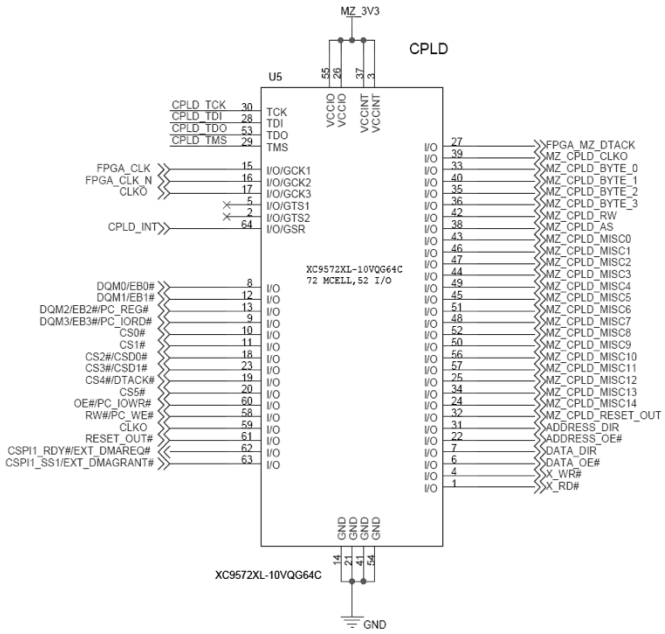
➢ **Interface from ARM to hardware**
  - Exclusively through Chip Select 1 & 5 memory regions
  - All TLL5000 peripherals must be accessed through the FPGA
  - The only direct connection to the ARM9 is
    - LCD, RS-232, USB, Ethernet

System Block Diagram

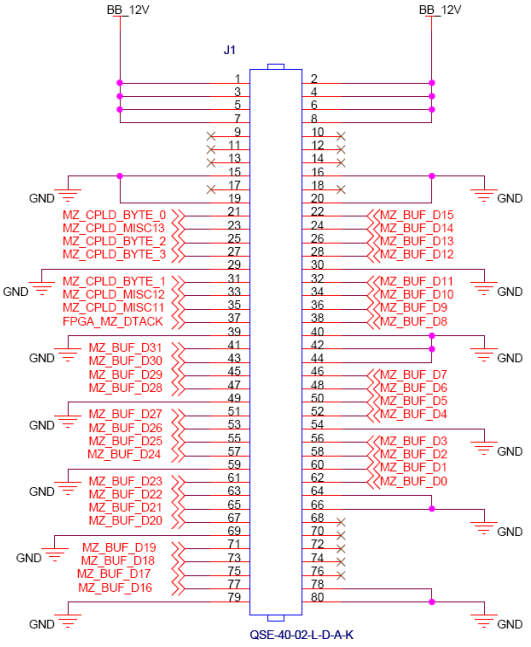


TLL6219 CPLD Connections

- **CPLD_INT connects to PF[16]**
- **MISC[xxxxx] signals defined by CPLD**
- **/DTACK for cycle timing**

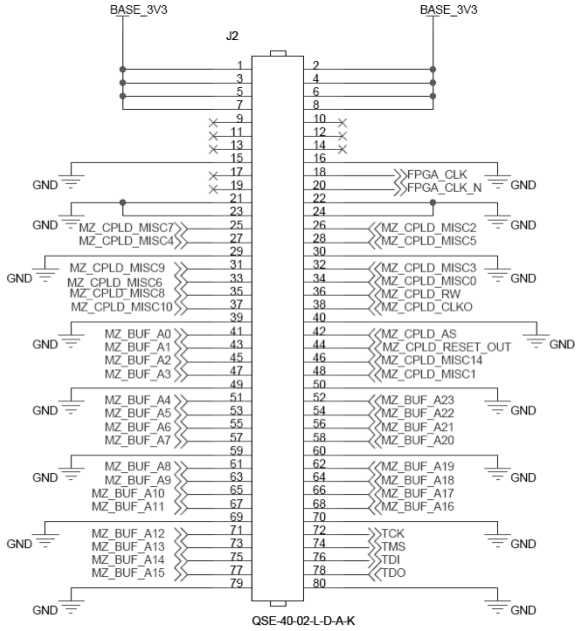


Connector A



MEZZANINE CONNECTOR I

Connector B



MEZZANINE CONNECTOR II

TLL6219 CPLD Overview

- **The CPLD generates read and write strobes for accesses in the /CS1 and /CS5 spaces (combinational logic)**
  - cs1_rs_b = ~(~cs1_b & ~oe_b);
  - cs1_ws_b = ~(~cs1_b & ~(&eb) & ~rw_b);
  - cs5_rs_b = ~(~cs5_b & ~oe_b);
  - cs5_ws_b = ~(~cs5_b & ~(&eb) & ~rw_b);
- **/DTACK is synchronized in the CPLD**
  - Single flip-flop synchronizer
- **Transceiver control**
  - The NFIO4 jumper controls data transceiver operation when the ARM is *not* accessing /CS1 or /CS5 space
    - If the jumper is NOT installed, the data transceivers are disabled
    - If the jumper IS installed, the data transceivers are enabled toward the FPGA to permit snooping bus activity not in the /CS1 or /CS5 spaces

TLL6219 CPLD_MISC[] Pins

mz_cpld_misc[0] = cs1_rs_b;	*/CS1 read strobe (active-low)*
mz_cpld_misc[1] = cs1_ws_b;	*/CS1 write strobe (active-low)*
mz_cpld_misc[2] = cs5_rs_b;	*/CS5 read strobe (active-low)*
mz_cpld_misc[3] = cs5_ws_b;	*/CS5 write strobe (active-low)*
mz_cpld_misc[4] = oe_b;	*from ARM926*
mz_cpld_misc[5] = cs0_b;	*from ARM926 (flash memory)*
mz_cpld_misc[6] = cs1_b;	*from ARM926 (FPGA access)*
mz_cpld_misc[7] = cs2_b;	*from ARM926 (SDRAM)*
mz_cpld_misc[8] = cs3_b;	*from ARM926 (Ethernet)*
mz_cpld_misc[9] = cs5_b;	*from ARM926 (FPGA access)*
mz_cpld_misc[10] = nfio4;	*TLL6219 jumper*
mz_cpld_misc[11] = nfio5;	*TLL6219 jumper*
mz_cpld_misc[12] = data_dir;	*TLL6219 transceiver control*
mz_cpld_misc[13] = data_oe;	*TLL6219 transceiver control*
mz_cpld_misc[14] = fpga_interrupt;	*FPGA IRQ to ARM926 PF[16]*

iMX21 External Interface Module (EIM)

- **The EIM permits fine-grained control of the bus interface**
  - Bus width
  - Timing of /CSx assertion/negation
  - Timing of /OE, /WE assertion/negation
  - Dead cycles between transfers
  - DTACK sensitivity and sampling
  - Byte enable behavior
  - Burst mode

iMX21 EIM Timing Example

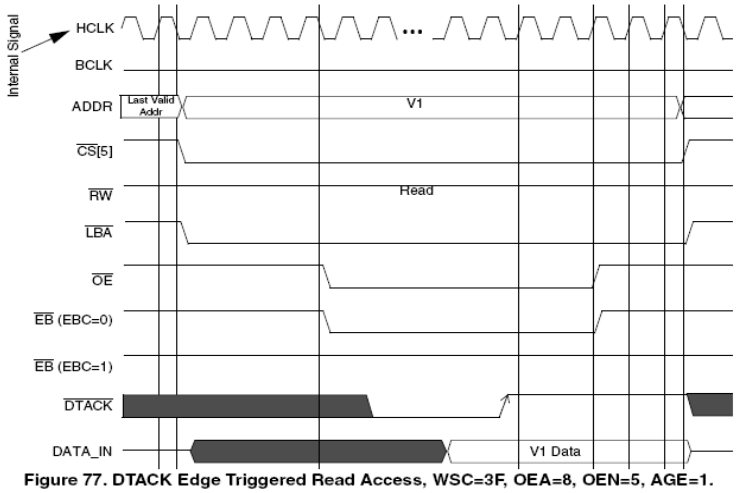


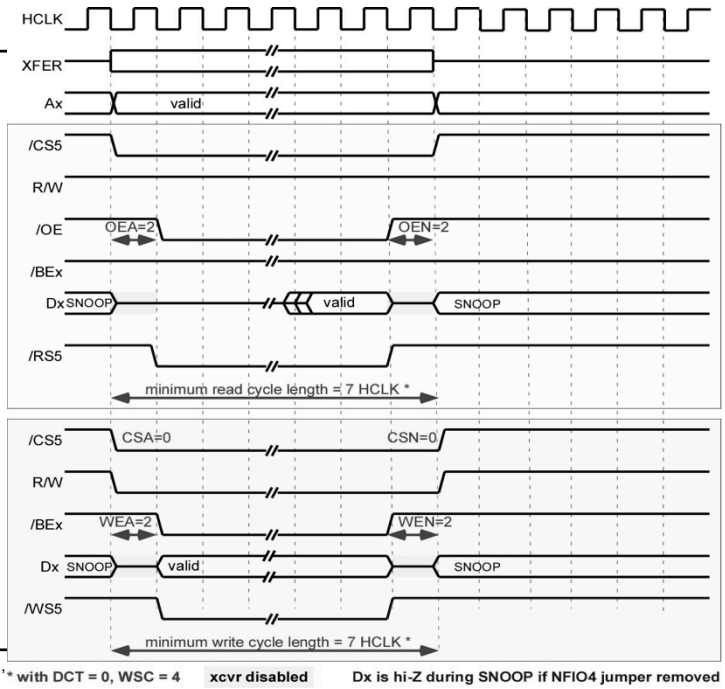
Figure 77. DTACK Edge Triggered Read Access, WSC=3F, OEA=8, OEN=5, AGE=1.

EIM Configuration in Boot Monitor

- **Chip Select 1 & 5 Upper Register settings in uMon**
  - CS1U,CS5U = 0x00000480
    - DCT = 0, at least 2 HCLK before /DTACK checked
    - RWA = 0, R/W asserted when address valid
    - WSC = 4 wait states (minimum cycle = 6 HCLK)
    - EW = 1, level sensitive /DTACK
- **Chip Select 1 & 5 Lower Register settings in uMon**
  - CS1L,CS5L = 0x22220E01
    - WEA = 2, byte enables asserted 2 half-clocks after start of access
    - WEN = 2, byte enables negated 2 half-clocks before end of access
    - OEA, OEN = 2, similar for /OE on reads
    - CSA = 0, /CS asserted when write starts
    - CSN = 0, /CS negated when write ends
    - EBC = 1, byte enables during writes only
    - DSZ = 6, 32-bit bus width
    - CSEN = 1, /CS enabled

Bus Timing

- **Default uMon settings**



* with DCT = 0, WSC = 4 xcvr disabled Dx is hi-Z during SNOOP if NFIO4 jumper removed