Motivation for Symbolic Trajectory Evaluation

- Equivalence checking between RTL and circuit schematics is difficult for some circuits (e.g., custom arrays)
  - Critical timing and self-timed control logic
  - Large number of bit-cells
  - Inherently complex sequential logic blocks
  - Dynamic logic
- Traditional tools fail on such circuits
  - Very large state space, too many initial state/input sequences for simulation-based tools
  - Boolean equivalence tools only check static cones of logic, do not capture dynamic behavior

Motivation

- Control for customer array structure

With zero delay functional simulation OUT is 0
- OUT pulse fans out to array READ/WRITE control signals
- Need to define unit delay for all gates to get a pulse on OUT
- Verification for correctness fails in downstream logic without this pulse

Symbolic Trajectory Evaluation

- Symbolic Trajectory Evaluation (STE) is a high-performance simulation-based model checking technique, originally invented by Seger and Bryant
- STE uses a combination of three-valued simulation and symbolic simulation

Example to illustrate STE

- The specification says that out represents the output of a 3-input AND gate with in0, in1, and in2 as inputs
- An implementation of the above spec
Scalar Simulation

- We need $2^n$ (8 here) simulation patterns
- One such pattern is the assertion
  - $(\text{in0 is 0}) \text{ and } (\text{in1 is 1}) \text{ and } (\text{in2 is 0}) \implies (\text{out is 0})$
- Every check like this is of the form $A \implies C$, where $A$ is an antecedent and $C$ is a consequent
- All STE assertions are of this form – we will give formal definition of STE assertions and define their semantics
- Not practical for large scale designs and so we need to make it more efficient, but how?

Three-valued Simulation

- Observation
  - Any input having assigned to 0, makes the output 0
  - Other inputs do not matter meaning could be 0 or 1 (X)
- If we introduce a new value (X = don’t care) in the simulation we need to evaluate the outputs of standard gates
Three-valued Simulation

- Cannot afford $2^n$ simulation patterns and so we will use 3-valued simulations
- Simulation pattern becomes
  - $(\text{in0 is 0}) \land (\text{in1 is X}) \land (\text{in2 is X}) \implies (\text{out is 0})$
  - This can be simplified into $(\text{in0 is 0}) \implies (\text{out is 0})$
  - Still of the form $A \implies C$
- Now the total number of simulations needed has reduced to $n + 1$ (4 here)
  - $(\text{in1 is 0}) \implies (\text{out is 0})$
  - $(\text{in2 is 0}) \implies (\text{out is 0})$
  - $(\text{in0 is 1}) \land (\text{in1 is 1}) \land (\text{in2 is 1}) \implies (\text{out is 1})$
- Can we do better?

Symbolic Simulation

- Assign symbols on inputs
- Now we need to do only one simulation
  - $(\text{in0 is a}) \land (\text{in1 is b}) \land (\text{in2 is c}) \implies (\text{out is a.b.c})$
- Can we do better than 1 simulation?
- No, but...
Checking for correctness

- Boolean expressions can be represented as BDDs (or other data structures) for performing constant time checks
- Verification steps to check the following assertion
  - \((\text{in}0 \text{ is } a) \text{ and } (\text{in}1 \text{ is } b) \text{ and } (\text{in}2 \text{ is } c) \implies (\text{out is } a.b.c)\)
- Implementation: From the antecedent assign symbols (equivalent to BDDs) to the inputs of the circuit
- Calculate the symbolic expressions (as BDDs) in the circuit nodes until the symbolic value of the output is known
- Specification: Calculate the consequent expression BDD
- Compare the two BDDs for equivalence
- Can we reduce the complexity of this one simulation?

Three-valued symbolic simulation

- In STE we combine the efficiency of three-valued simulation with the preciseness of symbolic simulations
- Use this combination by expressing the four 3-valued simulation runs as only one 3-valued symbolic simulation run
- Each assignment of 0 and 1 to two variables represents one 3-valued simulation run and since there are 4 possible assignments, and 4 3-valued simulation runs we can achieve this reduction (symbolic encoding)
- Symbolically,
  \[
  (((\neg p.\neg q) \rightarrow \text{in}0 \text{ is } 0) \text{ and } (\neg p.q) \rightarrow \text{in}1 \text{ is } 0) \text{ and } (p.\neg q) \rightarrow \text{in}2 \text{ is } 0) \text{ and } (p.q) \rightarrow (\text{in}0 \text{ is } 1) \text{ and } (\text{in}1 \text{ is } 1) \text{ and } (\text{in}2 \text{ is } 1))
  \implies (\text{out is } (p.q))
  \]
Three-valued symbolic simulation

- Assertion has the symbolic form \( P \rightarrow A \implies C \) where \( P \) is a Boolean expression (predicate)
- Logically, this is an implication
- Simulation-wise this assertion is going to assign values of nodes from \( A \) in situations where \( P \) is true otherwise, the nodes are kept at Xs

Dual-rail encoding

- The value of a 3-valued variable \( x \) can be represented by 2 Boolean variables \( x = (x_0, x_1) \)

<table>
<thead>
<tr>
<th>( x )</th>
<th>( (x_0, x_1) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>(1,0)</td>
</tr>
<tr>
<td>1</td>
<td>(0,1)</td>
</tr>
<tr>
<td>X</td>
<td>(0,0)</td>
</tr>
</tbody>
</table>

- Operators can be defined as follows
  - \( \neg x = \neg(x_0, x_1) = (x_1, x_0) \)
  - For 2 3-valued variables \( x = (x_0, x_1) \) and \( y = (y_0, y_1) \) we can calculate
    - \( \text{AND}: x \cdot y = (x_0, x_1) \cdot (y_0, y_1) = (x_0 + y_0), (x_1 \cdot y_1) \)
    - \( \text{OR}: x + y = (x_0, x_1) + (y_0, y_1) = (x_0 \cdot y_0), (x_1 + y_1) \)
So, this expression implies a few values for \(\text{in0}, \text{in1}, \text{in2}\):

\[
((\neg p \cdot \neg q) \rightarrow \text{in0 is 0}) \text{ and } \\
((\neg p \cdot q) \rightarrow \text{in1 is 0}) \text{ and } \\
((p \cdot \neg q) \rightarrow \text{in2 is 0}) \text{ and } \\
((p \cdot q) \rightarrow (\text{in0 is 1 and in1 is 1 and in2 is 1}))
\]

\[\implies (\text{out is } p \cdot q)\]

- If \((\neg p \cdot \neg q)\) then assign \(\text{in0}\) to 0
- Else if \((p \cdot q)\) then assign \(\text{in0}\) 1 else keep \(\text{in0}\) at an \(X\)
- Similar for \(\text{in1}\) and \(\text{in2}\)
- Since \(\text{in0}\) is a 3-valued variable its dual-rail encoding will be
  \[\text{in0} = ((\neg p \cdot \neg q), (p \cdot q))\]
- So, now the verification can be done by one simulation run with \([\log_2(n)]\) (2 here) number of variables

**Inaccuracy**

We have come from \(2^n\) simulations to one simulation using \([\log_2(n)]\) variables so what is the catch?

The \(\text{STE}\) assertion is

\[(\text{in0 is } a) \text{ and } (\text{in1 is } a) \implies (\text{out is } a)\]

Without specifying anything about \(\text{sel}\) in the antecedent it will be kept as an \(X\) making \(\text{out}\) \(X\).
Inaccuracy can be reduced by variables

The STE assertion that will resolve the issue is

\[(\text{sel is b}) \land (\text{in0 is a}) \land (\text{in1 is a}) \implies (\text{out is a})\]

Bottom line: there is a reduction in number of variables but under some circumstances one will need more variables for accuracy

STE Theory: information ordering

- X is “unknown (under-constrained) value of 0 or 1”
- T is “conflicting (over-constrained) value 0 and 1”
- The information ordering forms a lattice that can extend to \(n\) variables (\(X \leq 0, X \leq 1, 0 \leq T\) and \(1 \leq T\))
- Simulators need to use values \(V = \{0, 1, X, T\}\)
- Simulators use \(\neg T = T, x.T = T, T.x = T, x + T = T\) and \(T + x = T\)
- Logic gates are monotonic w.r.t. information ordering
Circuit model

- Set of circuit nodes is $N$ (example, in0, in1, out, the inputs and output of an AND gate)
- A state is an assignment of values from $V$ to circuit nodes, $s : N \rightarrow V$ (example, assignment $s$ (in0) = X, $s$ (in1) = 1, $s$ (out) = X)
- Circuit state is a collection of such values of the circuit nodes $S = (\forall n \in N : s(n))$ (example, $\langle X1X \rangle$)
- Note that in STE circuit state includes all nodes and not just latch nodes
- Closure function $F : S \times S$ (example, can be derived from the AND function extended to $V$)
  - Note that the closure function is not the same as the traditional next state function
  - $F$ propagates given values to other nodes
  - $F$ can be easily constructed from the netlist logic

Trajectory Evaluation Logic (TEL)

STE assertions are of the form $A \Rightarrow C$, where $A$ and $C$ are Trajectory Formulas in the language of TEL with the following syntax

Definition

$A, C ::= n \text{ is } 0$
  | $n \text{ is } 1$
  | $A_1 \text{ and } A_2$
  | $P \Rightarrow A$
  | $N \text{ A}$

Notes

- $P$ is a predicate over a set of symbolic variables $V$ that are time-independent
- The notion of time is in the form of the next time operator
- We can assign symbolic expressions to node values because ($n \text{ is } P$) is short form of ($P \Rightarrow n \text{ is } 1$) and ($\neg P \Rightarrow n \text{ is } 0$)
A Simplification and the Fundamental Theorem of STE

- The simulator performs one simulator run
- The simulator cannot check if $C$ holds for all trajectories
- It calculates the weakest trajectory $\sigma$ in which $A$ is satisfied and checks if $C$ holds on that particular trajectory
- By previous observation $C$ is going to hold on all trajectories that are stronger than $\sigma$
- This implies that it is enough to check $C$ only for the weakest trajectory satisfying $A$ instead of all trajectories

STE Example: Memory verification

- Memory with address width $k$ and data width $n$ needs $n \cdot 2^k$ state holding elements (state based model checkers)
- STE would need $n + k$ variables: let us see how
STE Example: Memory verification

Assertion for a memory
\[(\text{wr is } 1) \land (\text{addr}[0] \text{ is } a0) \land (\text{addr}[1] \text{ is } a1) \land (\text{in is } d) \land N ((\text{rd is } 1) \land (\text{addr}[0] \text{ is } a0) \land (\text{addr}[1] \text{ is } a1)) \implies N (\text{out is } d)\]

Observations
- Symbolic variables are \(a0, a1, d\) (total number is \(n + k\))
- Assertion starts from all Xs, writes into symbolic location \(a0a1\) with symbolic data \(d\) and then reads from the same symbolic location expecting to read out the symbolic data \(d\)

STE Example: Memory verification: time 0 and 1

Time 0: before the simulation begins all locations are Xs

Time 1: once written the symbolic values in the memory locations are
- loc0 // (“if I am addressed then I become \(d\) else I keep at X”)
  = if \((\neg a0.\neg a1 == \text{true})\) then new loc0 value is \(d\) else X
  = if \((\neg a0.\neg a1)\) then \(d\) else X
- loc1 = if \((\neg a0.a1)\) then \(d\) else X
- loc2 = if \((a0.\neg a1)\) then \(d\) else X
- loc3 = if \((a0.a1)\) then \(d\) else X
STE Example: Memory verification: time 2

Time 2: outputs are assigned depending on which location is read

- out0 // (“if I am addressed then value of loc0 else 0”)
  \[= \text{if } (\neg a_0.\neg a_1) \text{ then } \text{loc0 else 0}\]
  \[= \text{if } (\neg a_0.\neg a_1) \text{ then } (\text{if}(\neg a_0.\neg a_1) \text{ then } d \text{ else } X) \text{ else 0}\]
  \[= \text{if } (\neg a_0.\neg a_1) \text{ then } d \text{ else 0}\]
- Similarly, out1 = if (\neg a_0.a_1) then d else 0
- out2 = if (a_0.\neg a_1) then d else 0
- out3 = if (a_0.a_1) then d else 0

Simplifying, out = out0 OR out1 OR out2 OR out3 = d

Symbolic Trajectory Evaluation at Freescale

- VERSYS symbolic trajectory evaluation tool developed at Motorola/Freescale
  - Based on VOSS (from CMU/UBC)
- Trajectory formulas
  - Boolean expressions with the temporal next-time operator
  - Ternary values states represented by a Boolean encoding
- Properties of type: Antecedent \(\implies\) Consequent
  - Antecedent, Consequent are trajectory formulas
  - Antecedent sets up stimulus, state of the circuit
  - Consequent specifies constraint on the state sequence
- Used to verify PowerPC arrays at Motorola/Freescale in 8 – 10% of the design time
- Bugs found during array equivalence checking
  - Incorrect clock regenerators feeding latches
  - Control logic errors in READ/WRITE enables
  - Violation of “one-hot” property assumptions
  - Scan chain hookup errors
  - Potential circuit-related problems such as glitches and races
Other issues with STE

- LTL with finite number of next time $\mathbf{N}$ operators
- No notion of initial states
- No concept of reachable states

Term Rewriting Systems

- How a term can be rewritten/transformed into another
- Term rewriting for equivalence checking
- SMT solvers and application to verification and test
- Using term rewriting systems to design and verify processors
Term Rewriting Systems – Greatest Common Divisor

Euclid’s Algorithm
- Terms are functions of integers
- Four rules

Rules:
- Rule $R_1$: $\text{Gcd}(a, b)$ if $b \neq 0 \implies \text{Gcd}(b, \text{Rem}(a, b))$
- Rule $R_2$: $\text{Gcd}(a, 0) \implies a$
- Rule $R_3$: $\text{Rem}(a, b)$ if $a < b \implies a$
- Rule $R_4$: $\text{Rem}(a, b)$ if $a \geq b \implies \text{Rem}(a-b, b)$

Example:
- $\text{Gcd}(2,4) \overset{R_1}{\rightarrow} \text{Gcd}(4, \text{Rem}(2,4)) \overset{R_3}{\rightarrow} \text{Gcd}(4,2)$
- $\text{Gcd}(2,4) \overset{R_1}{\rightarrow} \text{Gcd}(2, \text{Rem}(4,2)) \overset{R_3}{\rightarrow} \text{Gcd}(2,2) \overset{R_4}{\rightarrow} 2$

Simple Arithmetic Rewriting

Terms
- integer, variable, (, ), +, *
- (Note: no evaluation rules defined)

Rules
- Rule1: $(op\ a\ b) \rightarrow (op\ b\ a)$ if $(b < a)$ and $op \in \{+,*\}$
- Rule2: $(+\ a\ b\ c) \rightarrow (+\ a\ c\ (+\ b\ c))$
- Rule3: $(+\ a\ a) \rightarrow (+\ a\ 2)$
- Rule4: $(op\ (op\ a\ b\ c)) \rightarrow (op\ (op\ a\ c\ b)\ b)$ if $(a < c \& c < b)$ and $op \in \{+,*\}$
- Rule5: $(op\ a\ (op\ b\ c)) \rightarrow (op\ (op\ b\ c\ a)\ a)$ if $(a > c \& b > c)$ and $op \in \{+,*\}$

Source: Shaun Feng
Example(s) in Rewriting

Example:
\[(\ast 4 (+ 3 3) \xrightarrow{\gamma} ((\ast 4 4) 3))\]
\[(\ast 4 (+ 3 3) \rightarrow ((\ast 4 4)) \rightarrow ((\ast 4 2) 3) \rightarrow ((\ast 2 3) 4))\]

Prove if
\[(\ast ((+ x y) y) \xrightarrow{\gamma} ((+ x x) y))\]

Term Rewriting Systems

- 3-tuple: \((T, L, R)\)
  - \(T\): Set of terms (functions, constants, variables, operators)
    \((t_1, t_2, \ldots, t_n)\)
  - \(L\): Set of labels \((R_1, R_2, \ldots)\)
  - \(R\): Set of labeled rules (may be conditional) \((r_1, r_2, \ldots, r_n)\)

- Rewrite process
  \[t_1 \xrightarrow{r_1} t_2 \xrightarrow{r_2} t_3 \xrightarrow{r_3} \ldots \xrightarrow{r_m} t_n \text{ (Normal Form)}\]
  - Term that cannot be rewritten any further
  - Depending on the system, several normal forms (or no normal form) may exist
  - Normal forms can be used for verification

Equivalence of two terms

- Determine whether the two terms have the same normal forms
- Undecidable in general
Rewriting 3NAND using 2NAND

Terms
2NAND(), A, B, C, a, b, ∧, ¬

Rules
- Rule R1: \( a \land b \rightarrow \neg 2NAND(a, b) \)
- Rule R2: \( \neg (\neg a) \rightarrow a \)
- Rule R3: \( \neg a \rightarrow 2NAND(a, a) \)

Apply the rules to get a 3NAND

\[ \neg((A \land B) \land C) \xrightarrow{R1} \neg(\neg 2NAND(A \land B, C)) \xrightarrow{R2} 2NAND(2NAND(2NAND(A, B), 2NAND(A, B)), C) \]

Termination and Cofluence

Termination
- No infinite rewriting sequence \( \rightarrow \) normal form exists

Cofluence
- Terms can be rewritten in multiple ways, but will eventually yield the same results
  - \( (*(+ 2 1) (+ 3 4)) \rightarrow (* 3 (+ 3 4)) \rightarrow (* 3 7) \)
  - \( (*(+ 2 1) (+ 3 4)) \rightarrow (* (+ 2 1) 7) \rightarrow (* 3 7) \)
- Normal form is unique if it exists

Convergence: Termination and Cofluence
- Normal form exists and is unique
- Convergent TRS used in equivalence checking
Rules of TRS Deduction

(I) Reflexivity: \( t \rightarrow t \)
(R) Replacement:
- R1: \( a \rightarrow a - 3 \) if \( a \in I \) and \( a \geq 3 \)

\[
\frac{t_k(x) \rightarrow t_a(x)}{t_k(x_0/x) \rightarrow t_a(x_0/x)}
\]
(C) Congruence
- R1: \( a \rightarrow a - 3 \) if \( a \geq 3 \)

\[
\frac{t_1 \rightarrow t'_1, \ldots, t_k \rightarrow t'_m}{f(t_1, \ldots, t_k) \rightarrow f(t'_1, \ldots, t'_k)}
\]
(T) Transitivity

\[
\frac{t_1 \rightarrow t_2, \ldots, t_2 \rightarrow t_3}{t_1 \rightarrow t_3}
\]

Checking Datapaths Using Arithmetic Expressions

Zhou, 1995
Based on Attribute Syntax Trees
Example: \(- (a * b * c) + b * c\)

(a) non-canonical form, and (b) canonical form under the lexicographic path ordering

Source: Zhou and Burleson, DAC 1995
Verification of Arithmetic Circuits using Term Rewriting

- RTL to RTL equivalence checking
- Verifies large multiplier designs
- Formalism: Term Rewriting Systems

Verifire
- Dedicated Arithmetic Circuit Checker
- Vtrans: Translates Verilog designs to Term Rewriting Systems
- Vprover: Proves equivalence of Term Rewriting Systems
  - Iterative engine which returns error trace if proof not found
  - Maintains an expanding rule base for expression minimization
  - Incomplete, but efficient, engine


RTL Equivalence Using Term Rewriting Systems (TRS)
Modeling Verilog as TRSs

- Verilog modules translated into *structural* TRS
- Resulting TRS “simulates” Verilog evaluation semantics
- TRS contains symbolic terms for signals in terms of other signals and primary inputs
- Symbolic terms (signal expressions) consist only of RTL operators

Verilog designs

- Every Verilog design corresponds to a TRS
- Every module is a term
- Inputs, Outputs, Reg, Wire, Module instantiations: Subterms
- Variable updating syntactic transformations: Rewrite rules (assignments, case, if-then-else statements)

Equivalence of TRSs

- Observation function applied to both TRSs to obtain *observed* set of terms
- Comparing entire symbolic values of terms: *intractable problem*
- Compare at intermediate stages of rewriting: *comparison points*
- Terms compared and expression equivalence proved at every comparison point
- Last comparison point: Normal form

Heuristic for comparison points: compute a partition of the bits for a particular output defined by the assignments to different subsets of bits of the same signal in both the reference (golden) and target designs
Checking Equivalence of Terms (reduce())

Check for equivalence between two symbolic terms by rewriting based on simplification

\[(x \& x) \rightarrow x\]
\[((x \& y) \& z) \rightarrow (x \& (y \& z))\]
\[(x \ll 3) \rightarrow (x \ll 2) + (x \ll 1) + (x \ll 1)\]
\[((x \ll 1) - x) \rightarrow x\]
\[((x \ll 1) \ll 1) \rightarrow (x \ll 2)\]

Equivalence of TRSs Applied to Arithmetic Circuits

- Observed Variables: Outputs
- Comparison points: Points where expressions for partial number of bits is obtained
- Bitwise equivalence of observed terms
- Normal form: Entire bitwidth compared

Example: checking ripple-carry adder against carry lookahead adder
Results on Multipliers

Different sizes of Wallace Tree Multipliers (Verilog RTL) compared with a simple Golden Multiplier (Verilog RTL) of the same size.

<table>
<thead>
<tr>
<th>Size</th>
<th>Verifire</th>
<th>Commercial Tool 1</th>
<th>Commercial Tool 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>4x4</td>
<td>14s</td>
<td>10s</td>
<td>9s</td>
</tr>
<tr>
<td>8x8</td>
<td>18s</td>
<td>18s</td>
<td>16s</td>
</tr>
<tr>
<td>16x16</td>
<td>25s</td>
<td>unfinished</td>
<td>unfinished</td>
</tr>
<tr>
<td>32x32</td>
<td>40s</td>
<td>unfinished</td>
<td>unfinished</td>
</tr>
<tr>
<td>64x64</td>
<td>60s</td>
<td>unfinished</td>
<td>unfinished</td>
</tr>
</tbody>
</table>

Distribution of Rewrite Rules for Multipliers Used by \texttt{reduce()}

<table>
<thead>
<tr>
<th>Rule class</th>
<th>Number of rules</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boolean</td>
<td>32</td>
<td>(x</td>
</tr>
<tr>
<td>Add/Subtract</td>
<td>44</td>
<td>(x + (y - z)) → ((x + y) - z)</td>
</tr>
<tr>
<td>Shift</td>
<td>16</td>
<td>(x &lt;&lt; 1) &lt;&lt; 1 → (x &lt;&lt; 2)</td>
</tr>
<tr>
<td>Multiplier Specific</td>
<td>9</td>
<td>(x &lt;&lt; 1) - x → x</td>
</tr>
<tr>
<td>Total</td>
<td>101</td>
<td></td>
</tr>
</tbody>
</table>
Comparison of Verifire Against Commercial Checker

<table>
<thead>
<tr>
<th>Multiplier</th>
<th>Verifire (Booth)</th>
<th>Commercial Tool (Booth)</th>
<th>Verifire (Wallace)</th>
<th>Commercial Tool (Wallace)</th>
<th>Verifire (Dadda)</th>
<th>Commercial Tool (Dadda)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4b x 4b</td>
<td>16s</td>
<td>12s</td>
<td>14s</td>
<td>10s</td>
<td>13s</td>
<td>8s</td>
</tr>
<tr>
<td>8b x 8b</td>
<td>19s</td>
<td>20s</td>
<td>18s</td>
<td>20s</td>
<td>17s</td>
<td>17s</td>
</tr>
<tr>
<td>16b x 16b</td>
<td>24s</td>
<td>1942s</td>
<td>25s</td>
<td>972s</td>
<td>29s</td>
<td>29s</td>
</tr>
<tr>
<td>32b x 32b</td>
<td>37s</td>
<td>not completed</td>
<td>40s</td>
<td>not completed</td>
<td>51s</td>
<td>83s</td>
</tr>
<tr>
<td>64b x 64b</td>
<td>53s</td>
<td>-</td>
<td>60s</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

The commercial equivalence checker was assisted by manual compare points (determined from the automatically extracted compare points in Verifire)

Use of TRS with SMT for Verifying Embedded Software

- Verify that two short code segments compute the same result
- Symbolically simulate modern VLIW
- Use TRS to simplify symbolic expressions
- Send query to decision procedure for proof
  - Verify equivalence between two code segments
  - Check conditions of rules to simplify memory term/expression

Dealing with Absence of Canonical Forms

- Difficult to reduce two equivalent symbolic expressions to a canonical form
  - If two program segments have different control flows, the expressions will be very different
- Solution: Use a decision procedure with SMT solvers

Applied to TI C62x VLIW DSP (can handle DSP assembly code)
Found mismatch in a packet example in TI CPU and ISA reference

Flow of the Technique

Boolean Satisfiability (SAT)

Is there an assignment to the $p_1, p_2, \ldots, p_n$ variables such that $\phi$ evaluates to 1?

Source: Barrett and Seshia, ICCAD tutorial, 1999
Satisfiability Modulo Theories

Is there an assignment to the $x, y, z, w$ variables such that $\phi$ evaluates to 1?

Source: Barrett and Seshia, ICCAD tutorial, 1999

SMT Tools and Constraints

Many Tools
- MathSAT
- MiniSmt
- Boolector
- SMT-RAT
- Yices

Quantifier-Free Subset of Logic
- Generally deal with formulas of first-order logic without quantifiers ($\forall, \exists$)

Theory of Equality and Uninterpreted Functions (EUF)
- Only property required is Congruence
- $x = y \implies f(x) = f(y)$
Data and Function Abstraction with EUF

Bit-vectors to Abstract Domain (e.g. \( \mathbb{Z} \))

\[
\begin{align*}
X_0 & \Rightarrow x \\
X_1 & \\
X_2 & \\
\vdots & \\
X_{n-1} & 
\end{align*}
\]

Functional units to Uninterpreted Functions

\[
a = x \land b = y \Rightarrow f(a, b) = f(x, y)
\]

Source: Barrett and Seshia, ICCAD tutorial, 1999