VLSI Design, Fall 2020

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Homework No. 4

Assigned October 6, 2020, due October 15, 2020

1. Problem 11.2 from the Exercises for Chapter 11 (page 494).

2. Problem 11.3 from the Exercises for Chapter 11 (page 495).

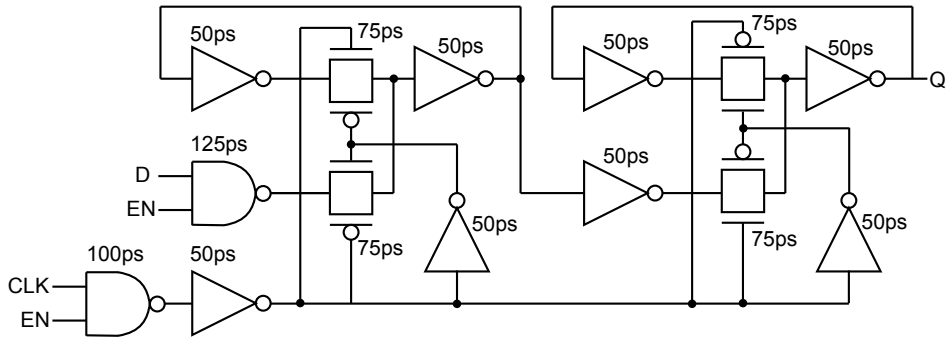
3. Problem 10.1 from the Exercises for Chapter 10 (pager 425).

4. Problem 10.2 from the Exercises for Chapter 10 (pager 425).

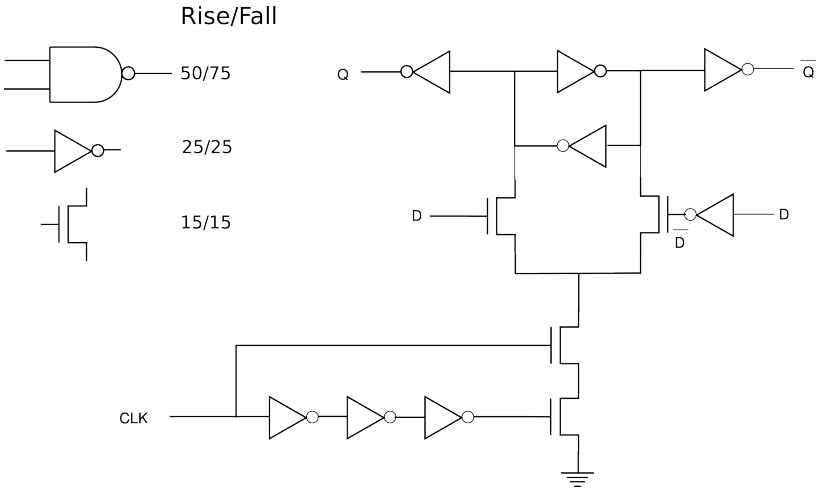
5. Problem 10.3 from the Exercises for Chapter 10 (pager 425).

6. Problem 10.4 from the Exercises for Chapter 10 (pager 425).

7. Find the setup, hold and clock-to-Q times of the flip-flop below; the delays of each component are indicated on the schematic.



8. (a) Find the setup time, hold time and clock-to-Q delay of the pulse-flip-flop below.



(b) Add one (or more) of the cells shown on the left of the flip-flop in (a) to reduce the setup time to 0 (or less), without changing the circuitry already in place. What is the new hold time and clock-to-Q delay?

(c) Add one (or more) of the cells shown on the left of the flip-flop in (a) to reduce the hold time to 0 (or less), without changing the circuitry already in place. What is the new setup time and clock-to-Q delay?