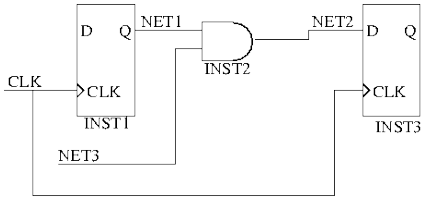
VLSI Design, Fall 2020

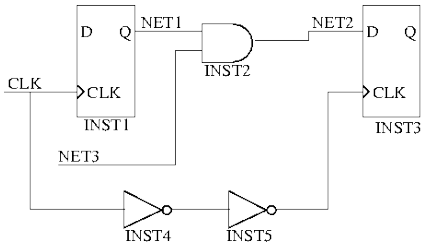
J. A. Abraham

Homework No. 5

Assigned October 15, 2020, due October 27, 2020

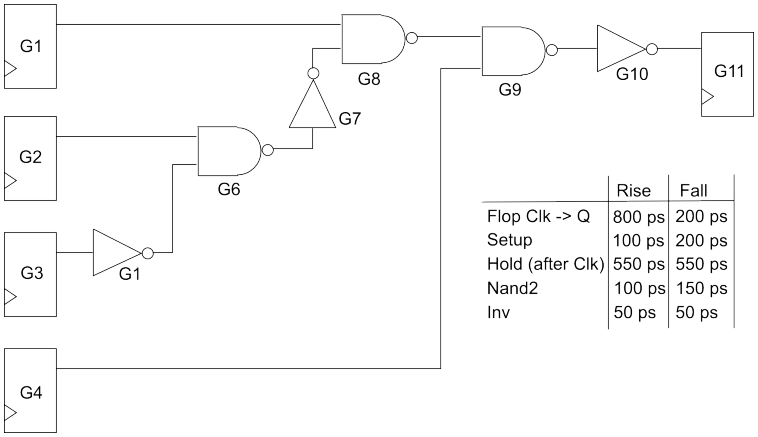
1. Identify if there are any hold time problems from INST1 to INST3 in the two circuits below If there are any, indicate by how much the hold time is violated. Indicate a solution to any hold-time violation.





	Rise	Fall
CLK → Q	500ps	500ps
Flop Hold Time	750ps	750ps
AND gate	300ps	200ps
Inverter	50ps	20ps

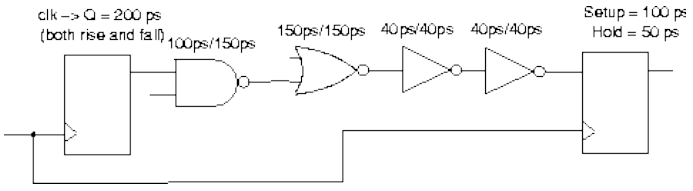
2. (a) Identify if there are any hold time problems from the source flops (G1, G2, G3 and G4) to G11 in the circuit below. If there are any, indicate by how much the hold time is violated and suggest a fix which minimizes the impact on the delay of the circuit. Use the delays from the table below.



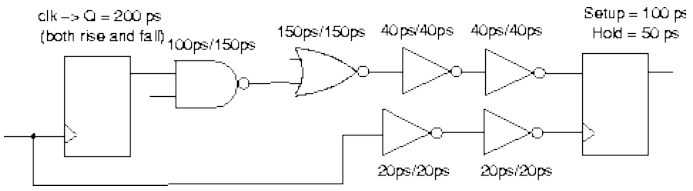
	Rise	Fall
Flop Clk -> Q	800 ps	200 ps
Setup	100 ps	200 ps
Hold (after Clk)	550 ps	550 ps
Nand2	100 ps	150 ps
Inv	50 ps	50 ps

(b) What is the maximum frequency of operation after fixing any hold-time violation?

3. (a) What is the maximum frequency at which the following design can operate?



(b) What is the maximum frequency at which the following design can operate?



4. Problem 9.31 from the Exercises for Chapter 9 (page 373).

5. Problem 9.33 from the Exercises for Chapter 9 (page 373).

6. Problem 9.35 from the Exercises for Chapter 9 (page 373).

Hint: Use a two stage design, a footless dynamic OR-AND-INVERT followed by a HI-skew Inverter.

7. Problem 9.37 from the Exercises for Chapter 9 (page 373).

8. Design a transistor level circuit realization of the following function using N-P Dynamic Logic. Assume you have two non-overlapping clocks ϕ and $\overline{\phi}$ and the restriction that you cannot use more than four transistors in series (including clocking transistors) in any path from an internal node to power or ground. You have only the uncomplemented inputs A, B, C, D, E, F, G, H available.

$Z = (A \cdot B + C \cdot D) \cdot (E \cdot F \cdot G + H)$

HINT: Realize two sub-functions using N-networks and feed the outputs of these sub-functions as inputs to a P-network.