VLSI Design, Fall 2020

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Homework No. 7

Assigned November 3, 2020, due November 10, 2020

1. Problem 5.1 from the Exercises for Chapter 5 (page 209).

2. Problem 5.2 from the Exercises for Chapter 5 (page 209).

3. Problem 5.4 from the Exercises for Chapter 5 (page 209).

4. Problem 5.5 from the Exercises for Chapter 5 (page 209).

5. Problem 5.6 from the Exercises for Chapter 5 (page 209).

6. An embedded hardware accelerator in a system-on-chip is designed in a 1 V, 90 nm process, and has 1 million logic transistors with an average width of 12λ. The gate capacitance, $C_g = 2$ fF/μm. The gates have an activity factor of 0.2.

(a) What is the maximum clock frequency if the dynamic power should not exceed 20 mW?

(b) If the subthreshold leakage is 20 nA/μm and the gate leakage is 2 nA/μm, and if half the transistors are off (on average), what is the leakage power?

7. (a) An ASIC uses a 65nm, 1V technology and has 500,000 gates, with 10,000 flip-flops connected in a scan chain using a Mux-Scan scheme as shown in Figure 1 below. The multiplexer has a propagation delay of 50 ps and a contamination delay of 30 ps. The flip-flop parameters are as follows.
CLK-Q: 40 ps
Setup time: 35 ps

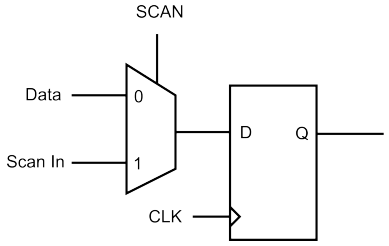

Figure 1: Mux-Scan Flip-Flop

How fast can the scan chain be clocked?

What is the maximum hold time allowable for the flip-flop at the above frequency?

What is the maximum hold time allowable for the flip-flop to enable the scan chain to be clocked at 1 GHz?

(b) The total gate length for the flip-flop (multiplexer and D-FF) is 7.5μm, and the average gate length for a gate in the combinational logic is 4μm. $C_g = 2fF/\mu m$. When the circuit is in scan mode, the combinational logic transitions have an activity factor of 0.2.

What is the power consumption of the circuit when the scan chain is clocked at 1GHz?

What is the clock speed for the power during scan to be kept below 500 mW?

If the subthreshold leakage is 15 nA/μm and the gate leakage is 0.1 nA/μm, on the average, what is the static power consumption of the ASIC?

8. A ring oscillator is made up of 15 inverters in a 65nm technology with a supply voltage of 1 V. Each inverter is minimum sized (2:1). The FO4 inverter delay for this technology is 30 ps. The gate capacitance is 2fF/μm.

What is the power consumption of the oscillator?

9. (a) Find a test for the node N stuck-at-0 in the circuit in Figure 2.

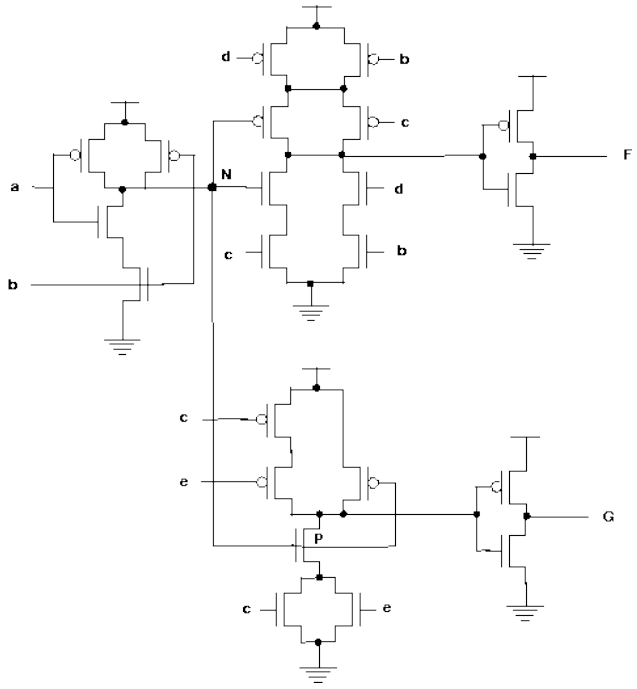

Figure 2: Test Generation

(b) Find the sequence of two tests which would detect that the nMOS transistor, labeled P, is slow to turn on.

10. Find test sequences $abcd \rightarrow abcd$ for the circuit in Figure 3 for the following faults.
(a) pMOS transistor with input b which is slow to turn on.
(b) nMOS transistor with input c which is slow to turn on.

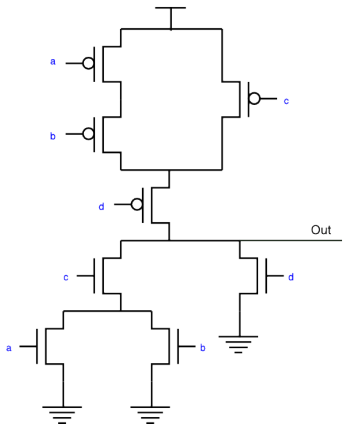

Figure 3: CMOS Complex Gate