1. Introduction, The CMOS Transistor

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VLSI Design
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Goals of This Course

Learn the principles of VLSI design

- Learn to design and implement state-of-the-art digital Very Large Scale Integrated (VLSI) chips using CMOS technology
- Understand the complete design flow
- Be able to design state-of-the-art CMOS chips in industry

Employ hierarchical design methods

- Use integrated circuit cells as building blocks
- Understand design issues at the layout, transistor, logic and register-transfer levels
- Use **Commercial Design Software** in the lab

Course Information

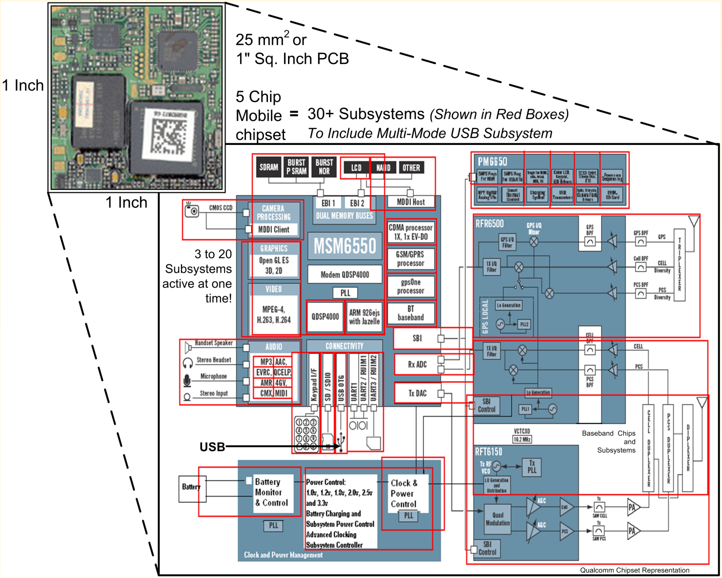
Instructor

- Jacob A. Abraham
- jaa@cerc.utexas.edu, +1-512-471-8983
- http://www.cerc.utexas.edu/~jaa/

More on the course

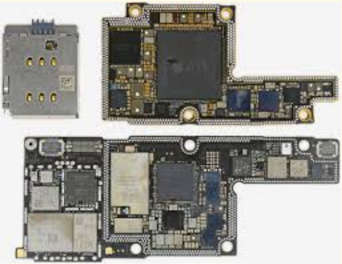
- Course Web Page (information duplicated on Canvas):
  - EE 382M: http://www.cerc.utexas.edu/~jaa/vlsi/
- Prerequisites: logic design, basic computer organization
- Textbook: Weste and Harris, CMOS VLSI Design: A Circuits and Systems Perspective, Addison Wesley/Pearson, 4th Edition, 2011
- Lectures and discussion in class will cover basic principles
- Homework, Laboratory exercises will help you gain a practical understanding of the subject

Example System-on-a-Chip (SoC)



From Chips on PCB to SoCs (ChipEstimate.com)

System Trends



iPhone X Teardown (techspot.com)

iPhone X board

Yesterday's science fiction (the "Tricorder" from *Star Trek*), tomorrow's medical diagnostic device

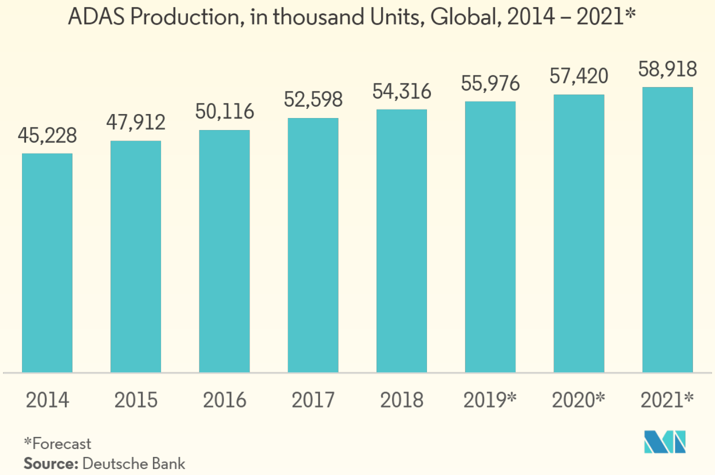
Where is this leading to?

New Opportunities

Source: Silicon Catalyst

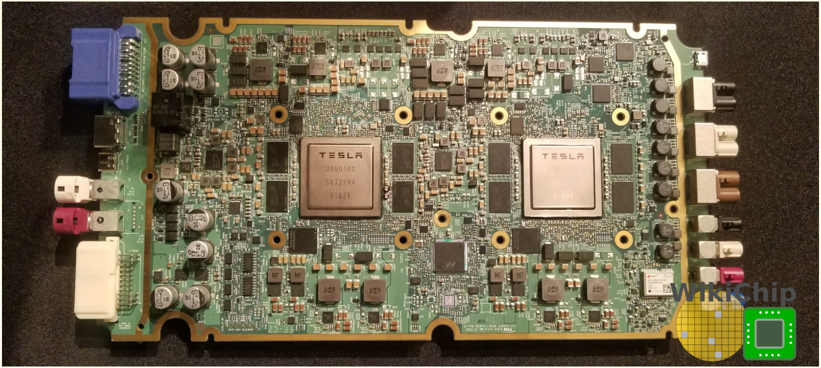
Projected Growth in Self-Driving Market

Advanced Driver-Assistance Systems



Estimates of 25 – 100 Billion IoT devices by 2020

Tesla's Neural Processor in the FSD Chip



fuse.wikichip.org

A Brief History of the Trnasistor

Some of the events which led to the microprocessor

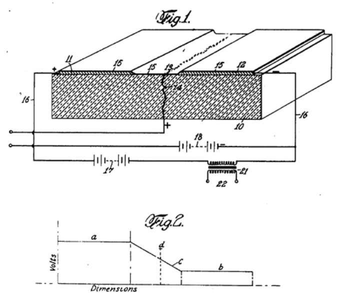
Photographs in the following are from “State of the Art: A photographic history of the integrated circuit,” Stan Augarten, Ticknor & Fields, 1983.

They can also be viewed on the Smithsonian web site, http://smithsonianchips.si.edu/

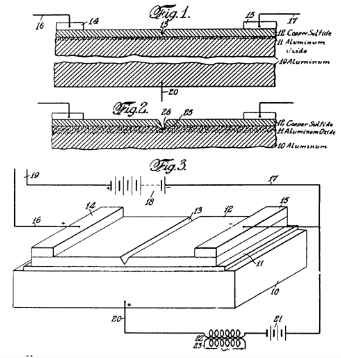
Early Ideas Leading to the Transistor

J. W. Lilienfelds patents

1930: "Method and apparatus for controlling electric currents," U.S. Patent 1,745,175

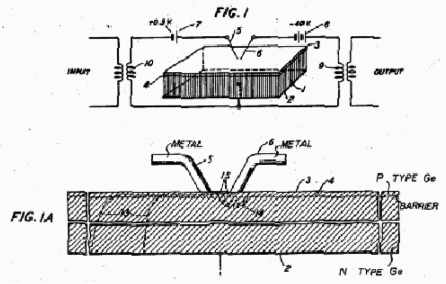


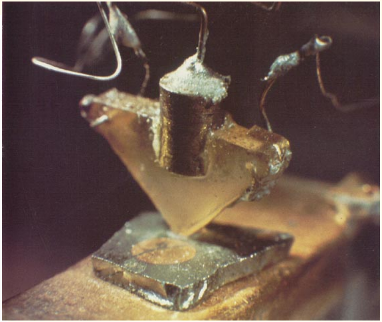
1933: "Device for controlling electric current," U. S. Patent 1,900,018



- 1940: Ohl develops the PN Junction
- 1945: Shockley's laboratory established
- 1947: Bardeen and Brattain create point contact transistor (U.S. Patent 2,524,035)

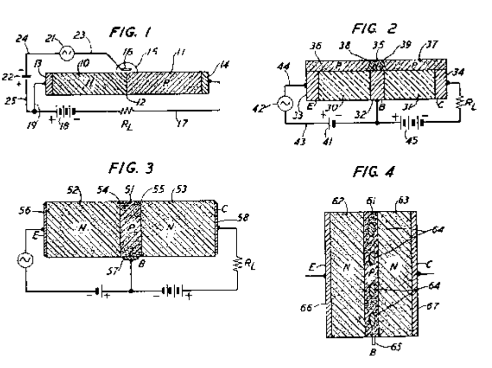
Diagram from patent application

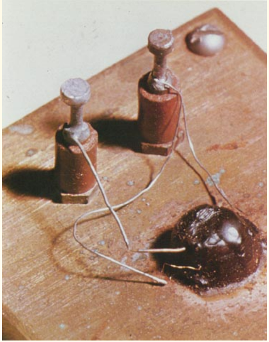




- 1951: Shockley develops a junction transistor manufacturable in quantity (U.S. Patent 2,623,105)

Diagram from patent application





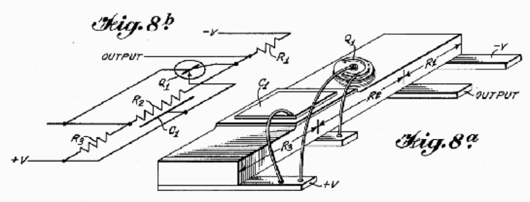
1950s Silicon Valley

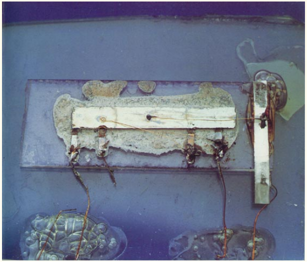
- 1950s: Shockley in Silicon Valley
- 1955: Noyce joins Shockley Laboratories
- 1954: The first transistor radio
- 1957: Noyce leaves Shockley Labs to form Fairchild with Jean Hoerni and Gordon Moore
- 1958: Hoerni invents technique for diffusing impurities into Si to build planar transistors using a SiO_2 insulator
- 1959: Noyce develops first true IC using planar transistors, back-to-back PN junctions for isolation, diode-isolated Si resistors and SiO_2 insulation with evaporated metal wiring on top

The Integrated Circuit (IC)

- 1958: Jack Kilby, working at TI, dreams up the idea of a monolithic “integrated circuit” (IC)
  - Components connected by hand-soldered wires and isolated by shaping, PN-diodes used as resistors (U.S. Patent 3,138,743)
- 1959: Robert Noyce, at Fairchild, independently develops the IC, solving many practical problems
- 2000: Kilby receives Nobel Prize in Physics (Noyce was no longer alive)

Diagram from Kilby patent application

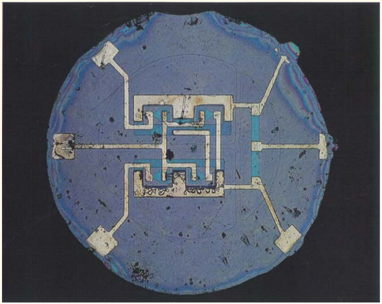




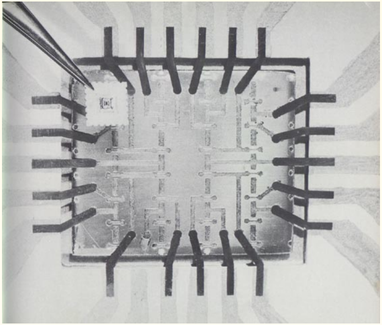
ICs, Cont'd

- 1961: TI and Fairchild introduce the first logic ICs ($50 in quantity)
- 1962: RCA develops the first MOS transistor

Fairchild Bipolar RTL Flop-Flop

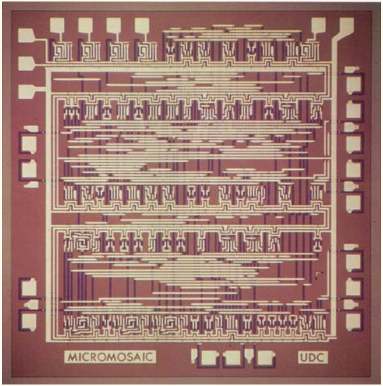


RCA 16-transistor MOSFET IC



Computer-Aided Design (CAD)

- 1967: Fairchild develops the Micromosaic IC using CAD
  - Final Al layer of interconnect could be customized for different application

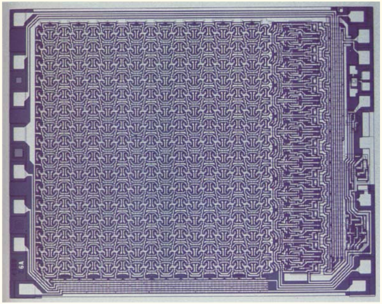


- 1968: Noyce, Moore leave Fairchild, start Intel

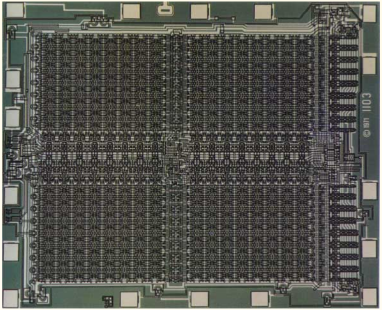
Static and Dynamic Random Access Memories (RAMs)

- 1970: Fairchild introduces the 4100, 256-bit Static Random Access Memory (SRAM)
- 1970: Intel starts selling a1K-bit Dynamic RAM (DRAM), the 1103

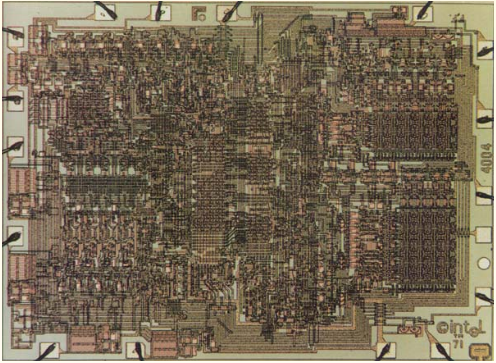
Fairchild 4100 256-bit SRAM



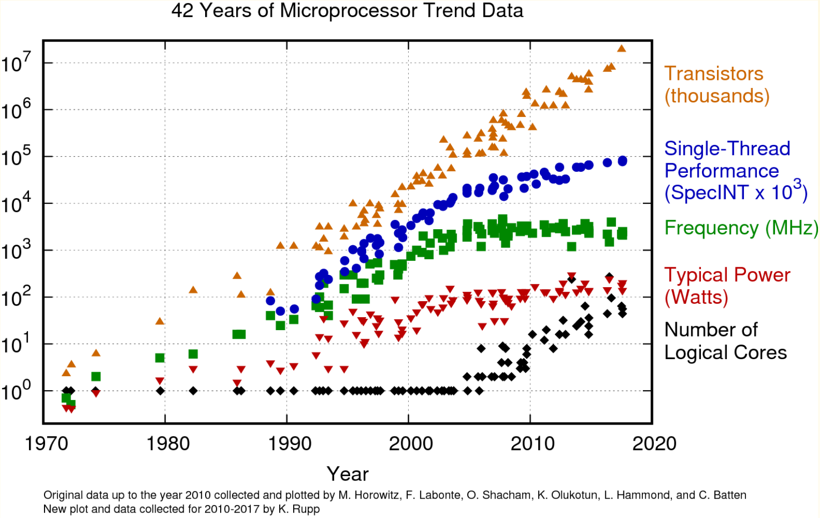
Intel 1103 1K-bit DRAM



- 1971: Intel introduces the first microprocessor, the 4004 (originally designed as a special circuit for a customer)



MOS Technology Trends – Moore's Law



Original data to 2010 by Horowitz et al. New data for 2010–2017 by K. Rupp

VLSI Design – The Big Picture

What do you do with a billion transistors?

- **Important to identify potential applications**
- Designing systems for a particular application:
  - Identify sub-functions
  - Design system using a variety of powerful Computer-Aided Design (CAD) tools
- Use a process relevant to industry
  - **Course developed with industry leaders in Austin**

Think of potential new applications

- Improving quality of life
  - Health
  - Education
  - Entertainment

Communication revolution (poor fisherman checking prices to decide where to sell)

Work in the Course

- Lectures
  - Read sections in text and slides before class
- Homework problems
  - Solve related problems posted every week
- Laboratory exercises
  - Three major exercises dealing with various aspects of VLSI design
  - Complete each section before the deadline
- Project (EE 382M)
  - Your opportunity to design a chip of interest to you
  - Design could be completed to the point where it could be fabricated by following process covered this course
- **Course involves a large amount of work throughout the semester**

Types of Integrated Circuit (IC) Designs

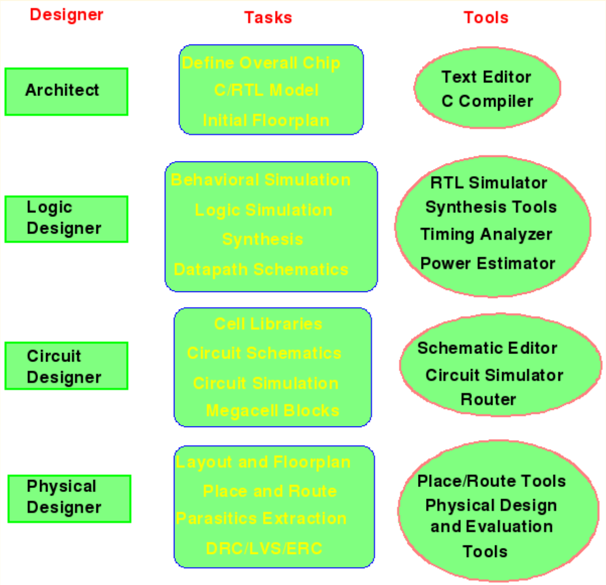
- IC Designs can be Digital (covered in this course), Analog, RF or mixed-signal

Digital designs

- Full Custom
  - Every transistor designed and laid out by hand
  - Used for memories, datapaths in high performance processors, etc.
- ASIC (Application-Specific Integrated Circuits)
  - Designs synthesized automatically from a high-level language description
- Semi-Custom
  - Mixture of custom and synthesized modules

This course will cover all these design techniques

Steps in Designing Hardware



Laboratory Exercises

Exercise 1: Design, layout and evaluation of a register file

- Use Cadence layout software, HSpice simulation

Exercise 2: Design and evaluation of an ALU with standard cell libraries

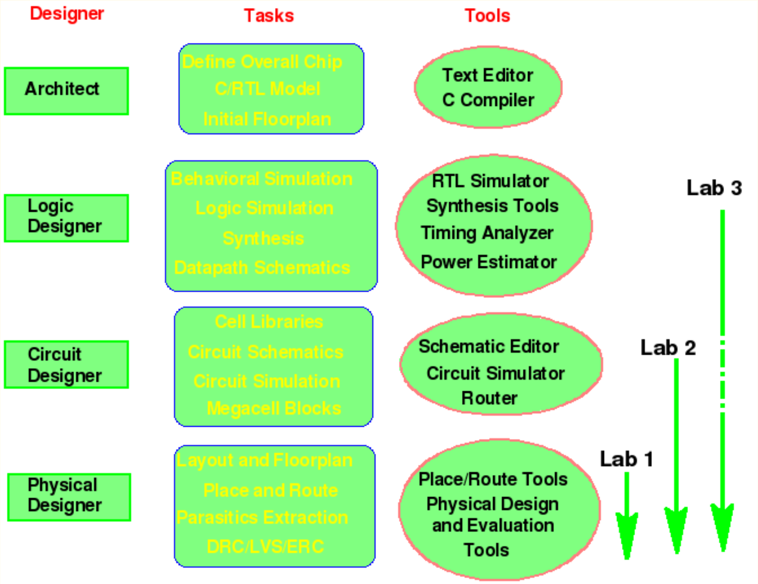
- Cadence schematic editor, Synopsys static timing analysis, Cadence place-and-route

Exercise 3: RT-level design and evaluation of bus controller

- Synopsys simulation, Synopsys synthesis, Cadence place-and-route

- **We will use an academic 45 nm standard cell library for the lab exercises**

Steps in Designing Hardware



Purpose of Laboratory Exercises

Mix of tools from different vendors mirrors industry practice

1. Familiarity with layout, circuit simulation, timing
2. Learn schematic design, timing optimization
3. Learn Register-Transfer level design, system simulation, logic synthesis and automatic place-and-route

Commercial CAD Tools

- Cadence, Synopsys
- Commercial software is powerful, but very complex
  - Designers sent to long training classes
  - Students will benefit from using the software, but we dont have the luxury of long training
  - TA has experience with the software
- Start work early in the lab
  - Unavailability of workstations is no excuse for late submissions
  - Plan designs carefully and save work frequently

Teaching Assistant and Laboratory

TA

- Akib Shah

Laboratory

- TA will hold demonstrations and discussion sessions
- Goal is to quickly learn the use of the tools
- Attend any session you wish
- You may need to go to your assigned section to demonstrate your laboratory exercise

Term Project (Graduate Students)

- Form 2 – 3 person teams
- Pick project
  - Based on something of interest to you
  - Discuss thoughts with me
  - Look at list of suggestions
- Complete design
- Evaluate design (for performance, power, etc.)
- Demonstrate operation
- Write report
- **Meet published deadlines**

Exams, Homework and Project

- Two exams, in class, open book and notes
- Final Exam (Undergraduates)
- Term project (Graduates)
- Penalty for late submission in labs: 5% per working day, maximum 25% (no submissions accepted after 5 working days)
- Bonus (for labs), early submission: 5% per working day (maximum 10%)
- Homework: work in teams
  - Homework due one week after it is posted (upload your work to Canvas
  - Submit one homework per "team", note all names on the sheet
  - Solutions will be posted on Canvas one week after problem set posted

Grading Policy

Grades will be absolute

- Grades based on demonstration of your knowledge of VLSI design
- Knowledge of fundamentals: homework, exams
- Practical application: laboratory exercises, project

Graduate Students

Homework	10%
Exams I and II	30%
Laboratory	45%
Term Project	15%

Undergraduate Students

Homework	10%
Exams I and II	25%
Laboratory	45%
Final Exam	20%

Academic Honesty

Develop professional ethics

- No cheating! This includes providing information about your work to, or receiving information from, another student
- Do not leave your work around for others to copy
- Protect your computer files
- Feel free to discuss homework, laboratory exercises with classmates, TAs and the instructors
- Homework exercises can be submitted by a team
- You can share knowledge of the tools
- However, do your designs and lab exercises by yourself and the submitted work should be your own

University Honor Code

https://law.utexas.edu/student-affairs/academic-services/policies-and-procedures/honor-code/

What Will You Learn?

- How integrated circuits work
- How to design chips with millions of transistors
  - Ways of managing the complexity
  - Use of tools to speed up the design process
- Identifying performance bottlenecks
- Ways of speeding up circuits
- Making sure the designs are correct
- Making the chips testable after manufacture
- Other issues: effect of technologies, reducing power consumption, etc.

Learning General Principles

- Chip design involves optimization, tradeoffs
- Need the ability to work as part of a group
- Technology changes fast, so it is important to understand the general principles which would span technology generations
- Systems are implemented using building blocks (which may be technology-specific)
    - Example: relays $\rightarrow$ tubes $\rightarrow$ bipolar transistors $\rightarrow$ MOS transistors (which are like relay switches) $\rightarrow$ Carbon nanotube transistor $\rightarrow$??
- **Lot of work in course, but you'll learn a lot**

Voltages and Logic Levels

Represent logic levels with different voltages

- Ground (GND, V_{SS}) $=$ 0V – can represent logic 0
- Power supply (V_{DD}) can represent logic 1

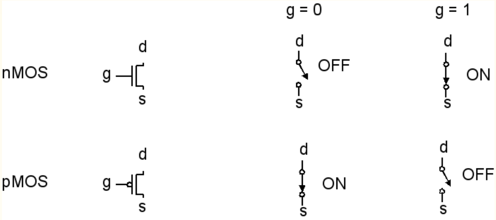
Decreasing voltages

- In 1980s, $V_{DD} =$ 5V
- V_{DD} has been decreasing in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- $V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, 0.9, \ldots$

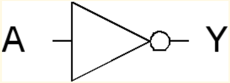
Metal Oxide Semiconductor (MOS) Transistors as Switches

Can view MOS transistors as electrically controlled switches

- Transistors we will use are built on a semiconductor with the control isolated from the semiconductor by an oxide
  - We'll see more of the MOS technology in the next class
- Two types of transistors, **nMOS** and **pMOS**
- The three terminals are gate (the control), source and drain
- Voltage (logic 0 or 1) on the gate controls source-drain path
- **The nMOS (pMOS) switch passes a 0 (1) well**
  - The voltages are degraded for the other values



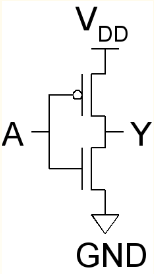
CMOS Inverter

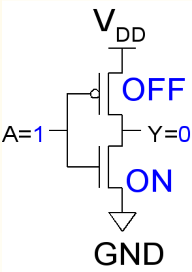


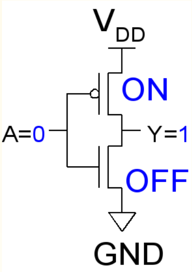
A	Y
0	
1	

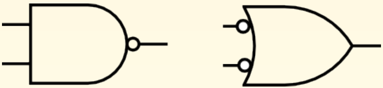
A	Y
0	
1	0

A	Y
0	1
1	0





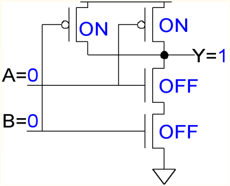


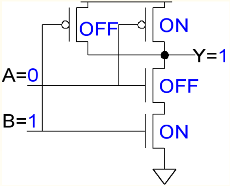


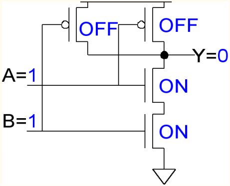
A	B	Y
0	0	1
0	1	
1	0	
1	1	

A	B	Y
0	0	1
0	1	1
1	0	
1	1	

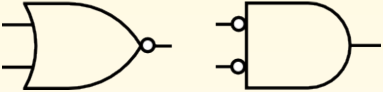
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



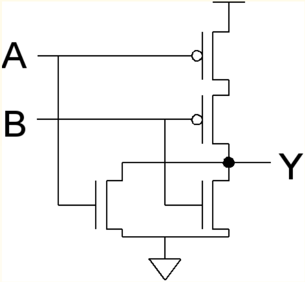




CMOS NOR Gate

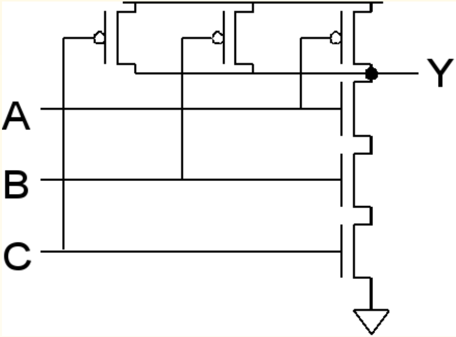


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



3-Input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0



Characteristics of CMOS Gates

In general, when the circuit is stable

- There is a path from one supply (V_{DD} or V_{SS}) to the output (low static power dissipation)
- There is NEVER a path from one supply to another

When circuit is switching

- There is a momentary drain of current when a gate switches from one state to the other
- Dynamic power dissipation

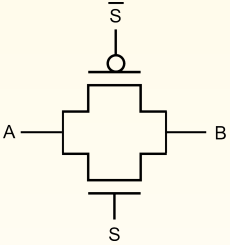
If a node has no path to power or ground, the previous value is retained due to the capacitance of the node

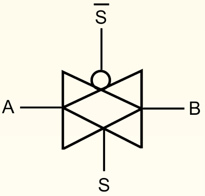
- Sometimes used as for dynamic storage

Complementary Switch (Transmission Gate)

Switch which does not degrade logic values

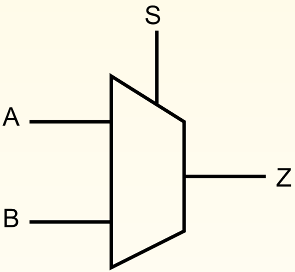
- Remember, the nMOS (pMOS) switch degrades a 1 (0)
- We'll analyze the electrical characteristics and see the reason for this next week
- Combine n- and p-channel switches in parallel to get a switch which passes both '1' and '0' well

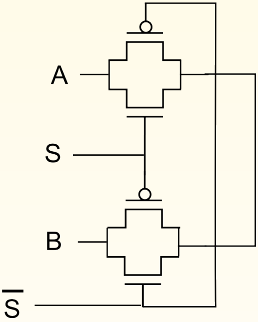




Two-input Multiplexer (MUX) using only switches

A	B	S	$\overline{S}$	Z	
X	0	0	1	0	B
X	1	0	1	1	
0	X	1	0	0	A
1	X	1	0	1	

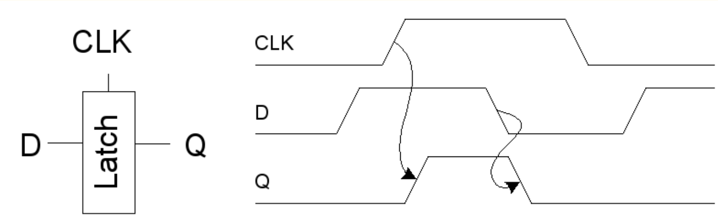




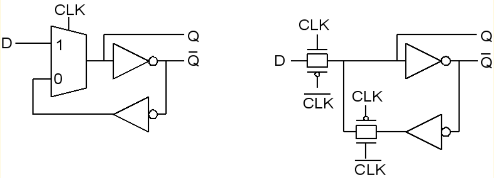
D Latch

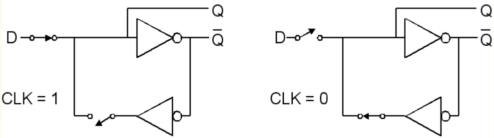
Basic Memory Element

- When CLK = 1, latch is transparent
  - D flows through to Q like a buffer
- When CLK = 0, the latch is opaque
  - Q holds its old value independent of D
- a.k.a., **transparent latch** or **level-sensitive latch**

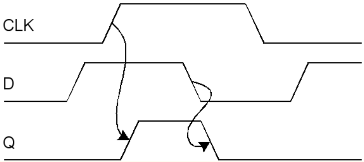


D Latch Design: MUX chooses between D and old Q

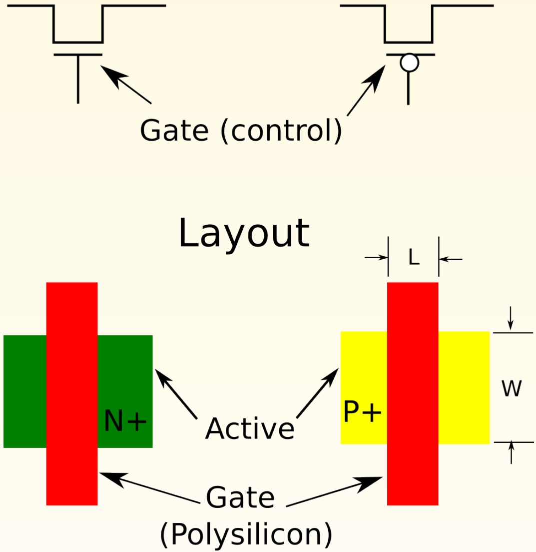




D Latch Operation



Layout – Implementing Transistors and Interconnect in Silicon

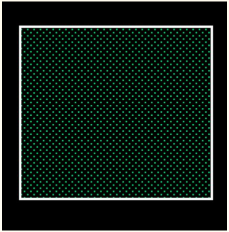


Laying Out an nMOS Transistor in Cadence

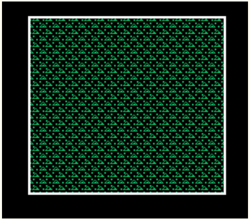
Transistors are implemented by layers

- pwell, active, nimplant, poly, metal1 and contact
  - Basic transistor (gate, source drain) implemented with active, nimplant and poly
  - pwell isolates transistors from other transistors – achieved with ties to appropriate potentials (power or ground)
  - contact connects nodes of the transistors to other nodes via metal

Active layer

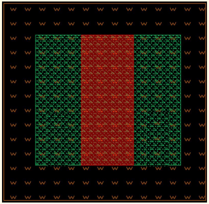


Implant layer

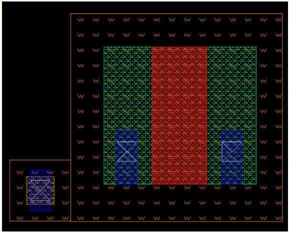


Gate and Contacts

nMOS Transistor with p-Well



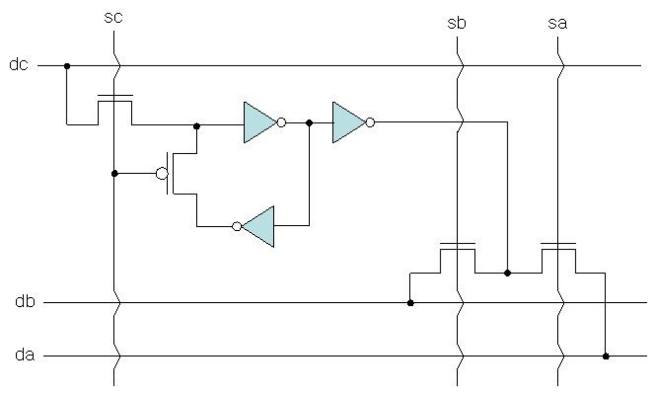
Transistor with Contacts (Source, Drain, Body)



Lab. 1 – 1-bit SRAM, 4 × 4 Array

Evaluation criteria: (a) Correct operation, (b) Area

1-bit memory cell



"Tile" this cell to make a 4 × 4 array

Evaluate performance of the array, with decoder