7. Combinational Circuits

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Support for Students

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Review: Logical Effort, Gates and Paths

Term	**Stage**	**Path**
Number of stages	1	N
Logical effort	g	$G = \prod g_i$
Electrical effort	$h = \frac{C_{out}}{C_{in}}$	$H = \frac{C_{out-path}}{C_{in-path}}$
Branching effort	$b = \frac{C_{on-path}+C_{off-path}}{C_{on-path}}$	$B = \prod b_i$
Effort	f = gh	F = GBH
Effort delay	f	$D_F = \sum f_i$
Parasitic delay	p	$P = \sum p_i$
Delay	d = f + p	$D = \sum d_i = D_F + P$

Steps in Logical Effort

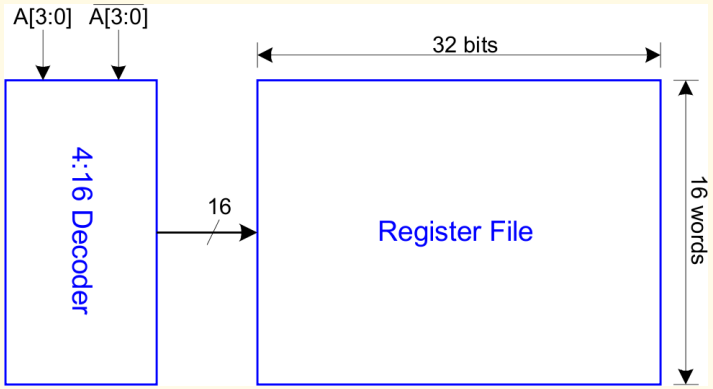
1. Compute path effort $F = GBH$
2. Estimate best number of stages $N = \log_4 F$
3. Sketch path with N stages
4. Estimate least delay $D = NF^{\frac{1}{N}} + P$
5. Determine best stage effort $\hat{f} = F^{\frac{1}{N}}$
6. Find gate sizes $C_{in} = \frac{g_i C_{out}}{f}$

Limits of logical effort

- Chicken and egg problem
  - Need path to compute G
  - But, don't know number of stages without G
- Simplistic delay model, neglects input rise time effects
- Interconnect
  - Iteration required in designs with significant wires
- Maximum speed only
  - Not minimum area/power for constrained delay

Review: Decoder Example, Number of Stages

- 16 word, (32 bit) register file
- Each bit presents load of 3 unit-sized transistors
- True and complementary address inputs A[3:0]
- Each input may drive 10 unit-sized transistors



Find: number of stages, sizes of gates, speed

- Decoder effort is mainly electrical and branching
  - Electrical Effort: H = (32*3)/10 = 9.6
  - Branching Effort: B = 8
- If we neglect logical effort (assume G = 1)
  - Path Effort: F = GBH = 76.8
- Number of Stages: $N = \log_4 F = 3.1$
- Try a 3-stage design

Decoder Review: Gate Sizes and Delay

Logical Effort: G = 1 * 6/3 * 1 = 2

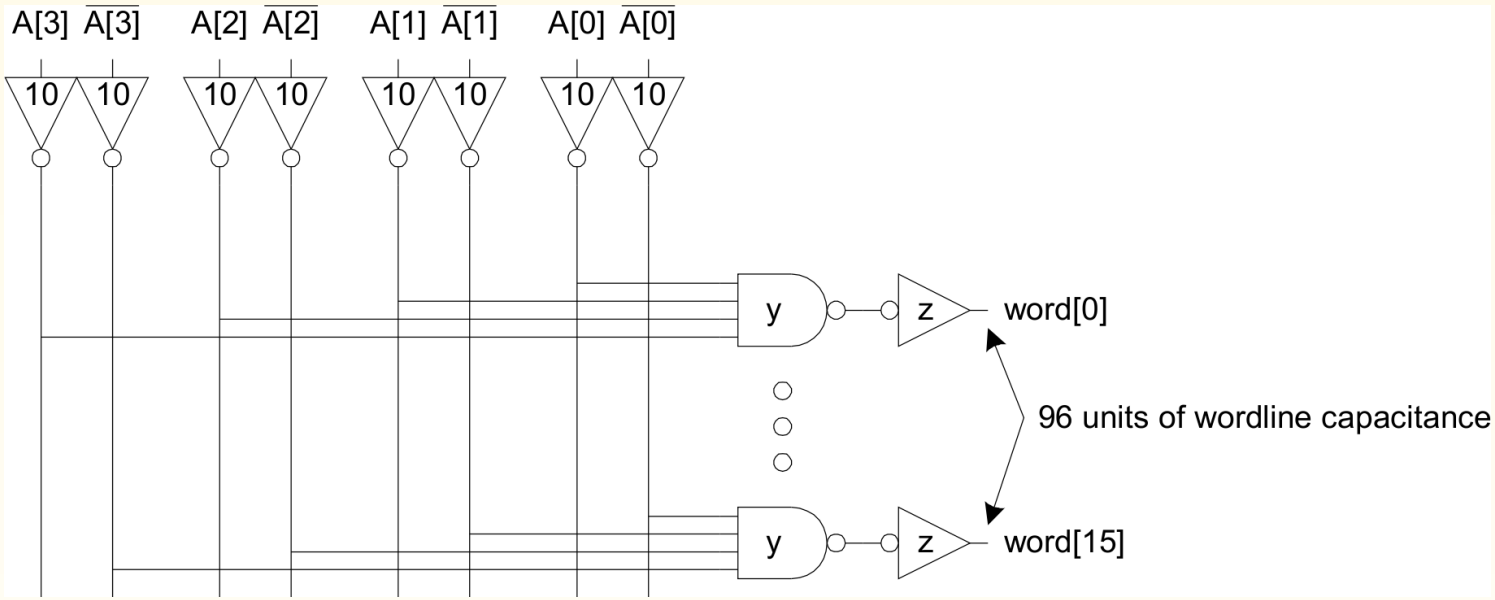
Path Effort: F = GBH = 154

Stage Effort: $\hat{f} = F^{\frac{1}{3}} = 5.36$

Path Delay: $D = 3\hat{f} + 1 + 4 + 1 = 22.1$

Gate sizes: z = 96*1/5.36 = 18

Gate sizes: y = 18*2/5.36 = 6.7



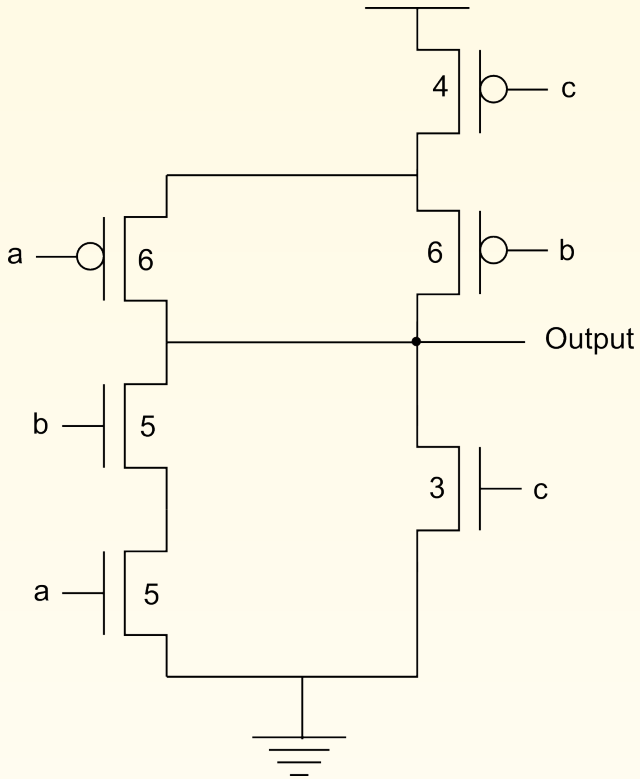
Decoder Review: Comparison

Compare many alternatives with a spreadsheet

Design	**N**	**G**	**P**	**D**
NAND4-INV	2	2	5	29.8
NAND2-NOR2	2	20/9	4	30.1
INV-NAND4-INV	3	2	6	22.1
NAND4-INV-INV-INV	4	2	7	21.1
NAND2-NOR2-INV-INV	4	20/9	6	20.5
NAND2-INV-NAND2-INV	4	16/9	6	19.7
INV-NAND2-INV-NAND2-INV	5	16/9	7	20.4
NAND2-INV-NAND2-INV-INV-INV	6	16/9	8	21.6

Review: Logical Effort Example

Find the logical efforts for the inputs, a, b, and c in the circuit below.



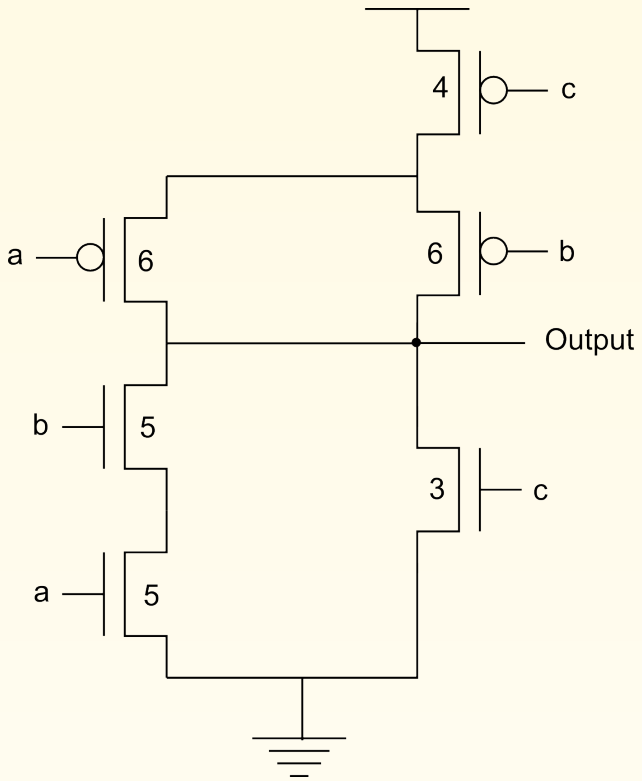
Output

	Rising	Falling
a		
b		
c		

Suggest a way to reduce the parasitic delay of this circuit by modifying the structure (but keeping the same function).

Example, Cont'd

Find the logical efforts for the inputs, a, b, and c in the circuit below.

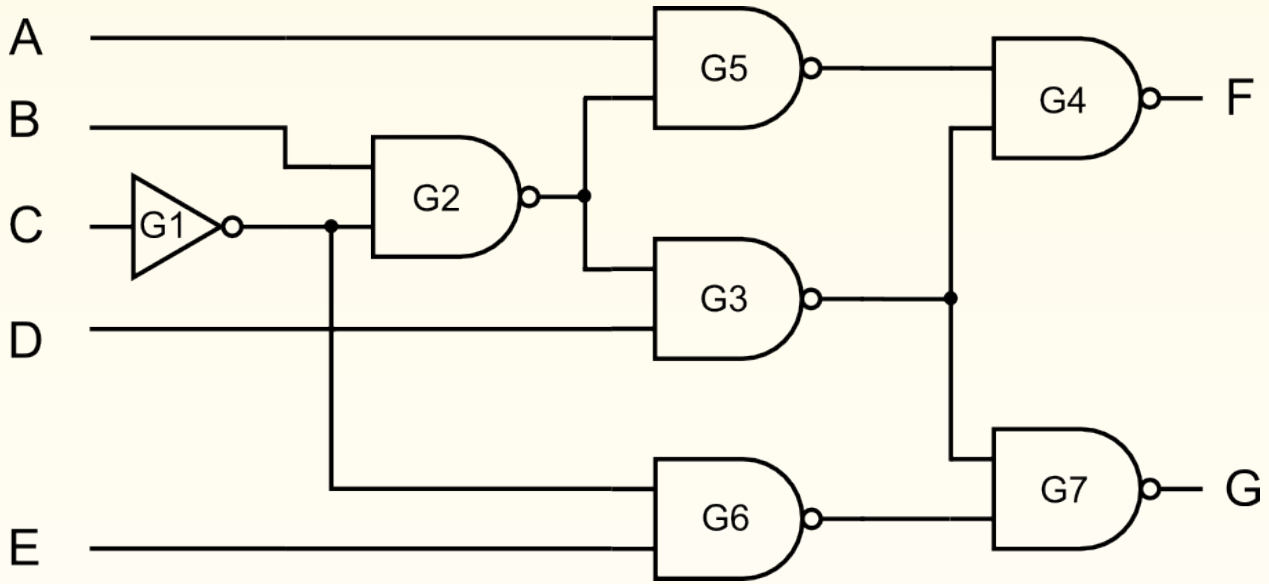


	Output	
	Rising	Falling
a	55/18	22/15
b	55/18	22/15
c	35/18	7/9

To reduce the parasitic delay of this circuit, swap the parallel combination of pMOS transistors with inputs a, b with the pMOS transistor with input c

Example: Sizing Paths

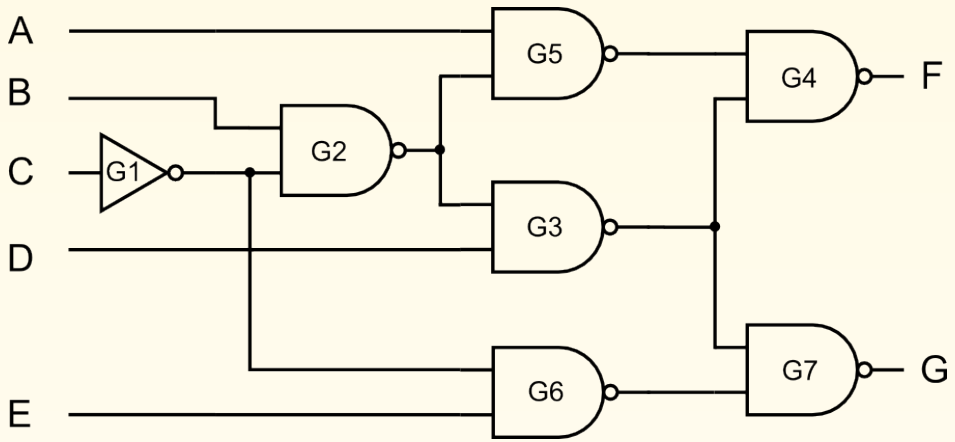
Size the path G1-G2-G3-G4 in the circuit below using logical effort
Find the minimum delay and give the sizes of the P and N transistors to achieve this delay
Assume that the off-path capacitance is the same as the on-path capacitance for each branch
Input capacitance of Inverter G1 = 3 units.
Load capacitance driven by Gate G4 = 52 units.



Sizing Paths, Cont'd

Size the path G1-G2-G3-G4 in the circuit
Input capacitance of Inverter G1 = 3 units.
Load capacitance driven by Gate G4 = 52 units.

Delay = $\boxed{4.8}$ FO4 units



Sizes of transistors:

Gate	P	N
Gate G4	8	8
Gate G3	5	5
Gate G2	3	3
Gate G1	2	1

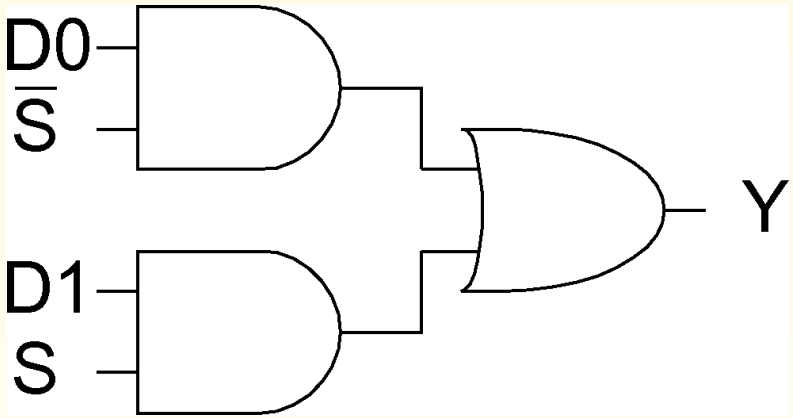
Delay of the path from A through gates G5 and G4 (assuming the input from G2=1 and D=0): $\boxed{2.08}$ FO4 units

Example of "Bubble Pushing"

Implement the circuit described by the code below

```
module mux(input s, d0, d1,
           output y);
assign y = s ? d1 : d0;
endmodule
```

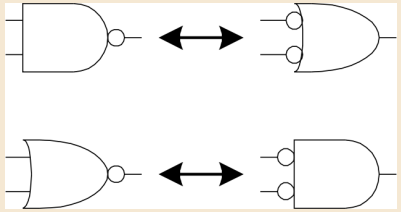
The specifications are easily met with a design using AND, OR and NOT gates

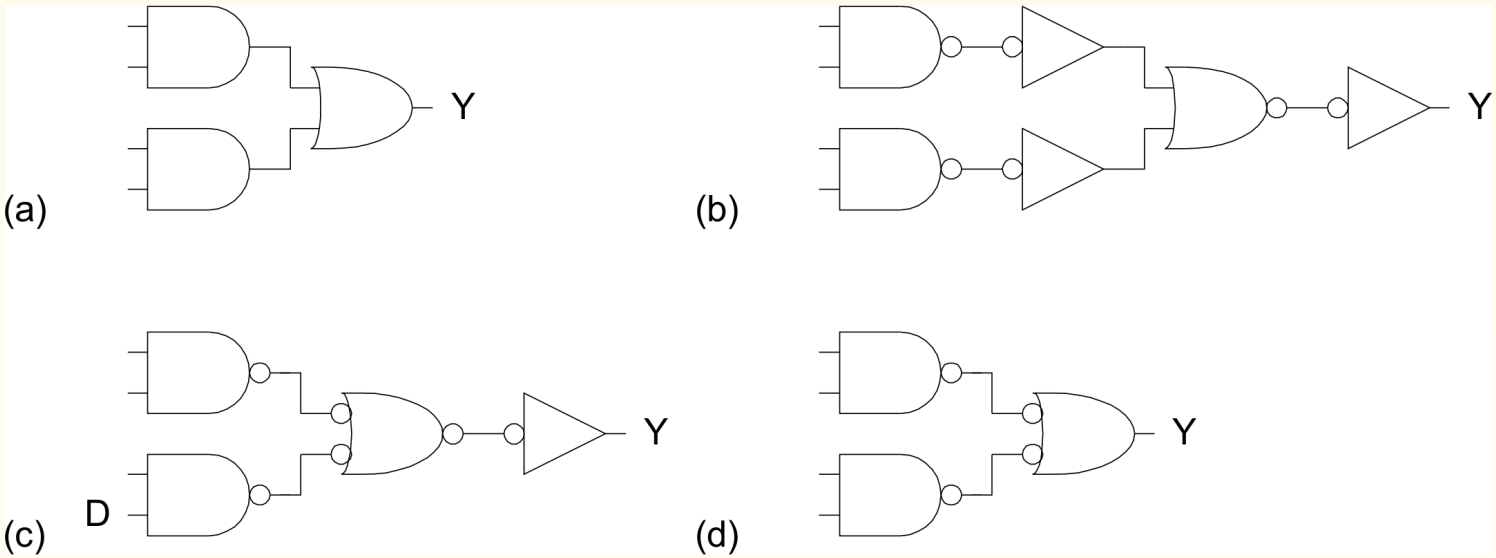


Convert to Design using NAND/NOR/NOT Gates

Bubble Pushing

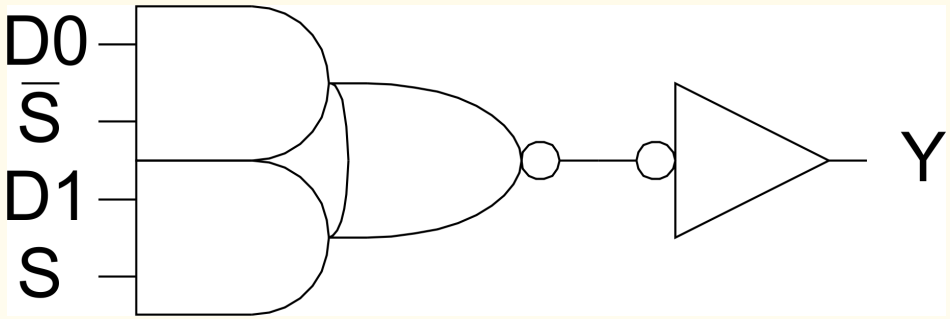
Start with network of AND/OR gates
Convert to NAND/NOR + inverters
Push bubbles around to simplify logic
Use DeMorgan's Law

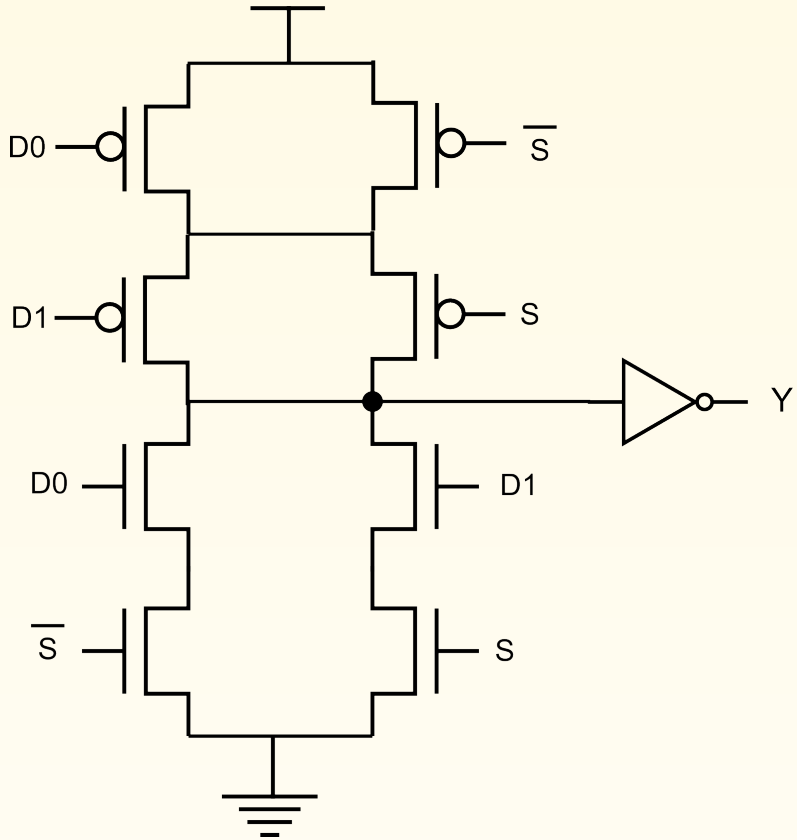




Example, Continued

Now, design the circuit with one compound gate and one inverter. Assume that $\bar{S}$ is available

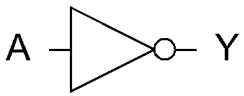


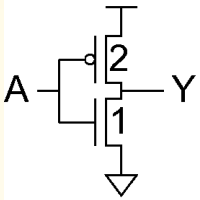


Compound Gates

Unit Inverter

$Y = \overline{A}$



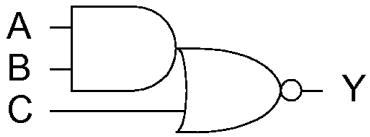


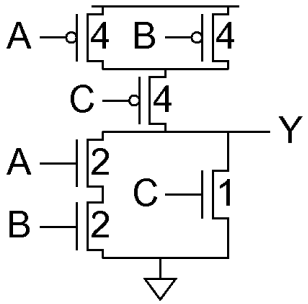
$g_A = 3/3$

$p = 3/3$

AOI21

$\overline{Y = A \cdot B + C}$





$g_A = 6/3$

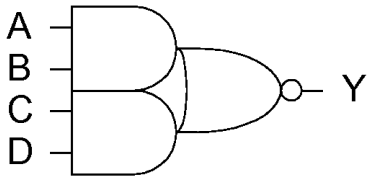
$g_B = 6/3$

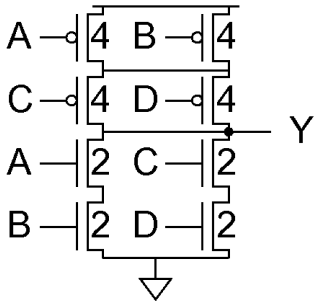
$g_C = 5/3$

$p = 7/3$

AOI22

$\overline{Y = A \cdot B + C \cdot D}$





$g_A = 6/3$

$g_B = 6/3$

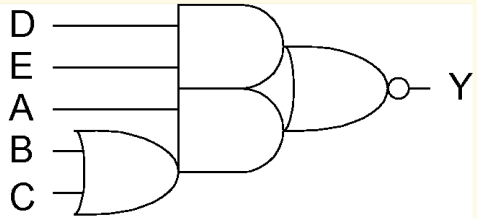
$g_C = 6/3$

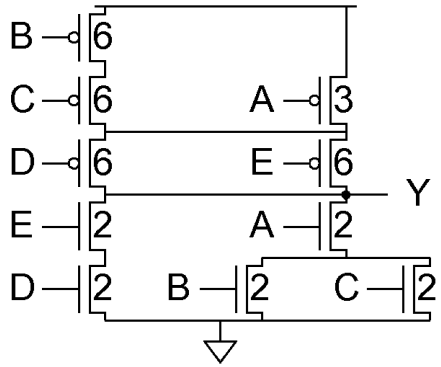
$g_D = 6/3$

$p = 12/3$

Complex AOI

$\overline{Y = A \cdot (B + C) + D \cdot E}$





$g_A = 5/3$

$g_B = 8/3$

$g_C = 8/3$

$g_D = 8/3$

$g_E = 8/3$

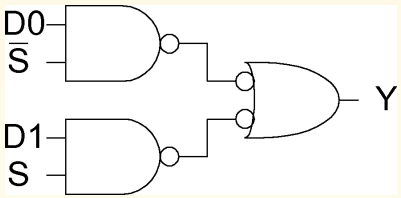
$p = 16/3$

Another Example

A multiplexer has a maximum input capacitance of 16 units on each input. It must drive a load of 160 units

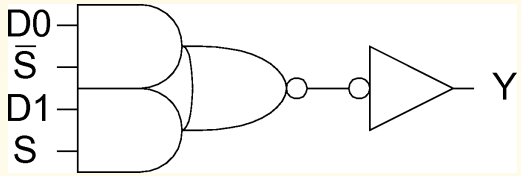
Estimate the delay of the NAND and compound gate designs

NAND Solution



$H = 160/16 = 10$
$B = 1$
$N = 2$
$P = 2 + 2 = 4$
$G = (4/3) \cdot (4/3) = 16/9$
$F = GBH = 160/9$
$\hat{f} = \sqrt[N]{F} = 4.2$
$D = N\hat{f} + P = 12.4\tau$

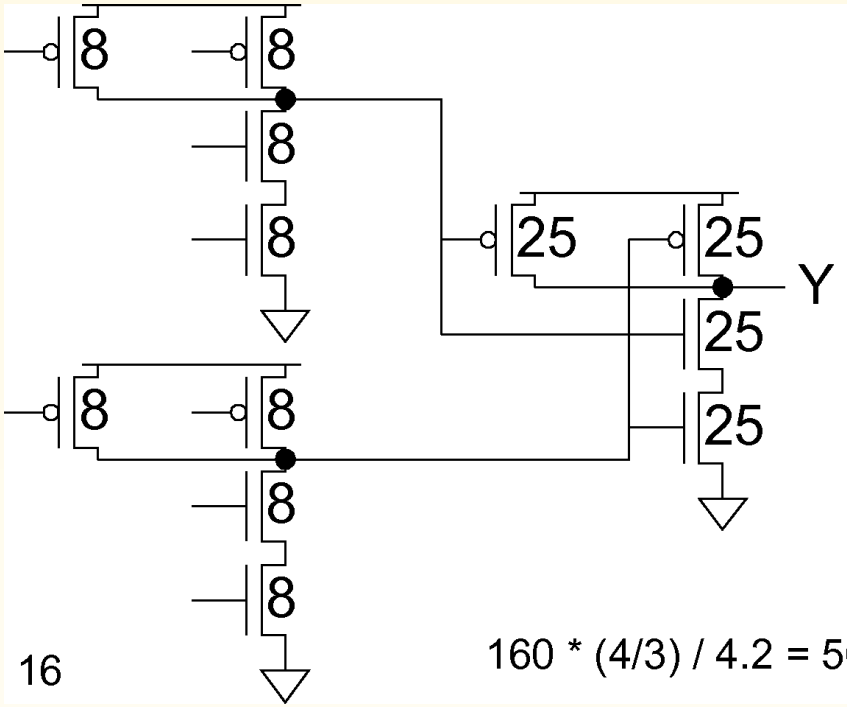
Compound Solution

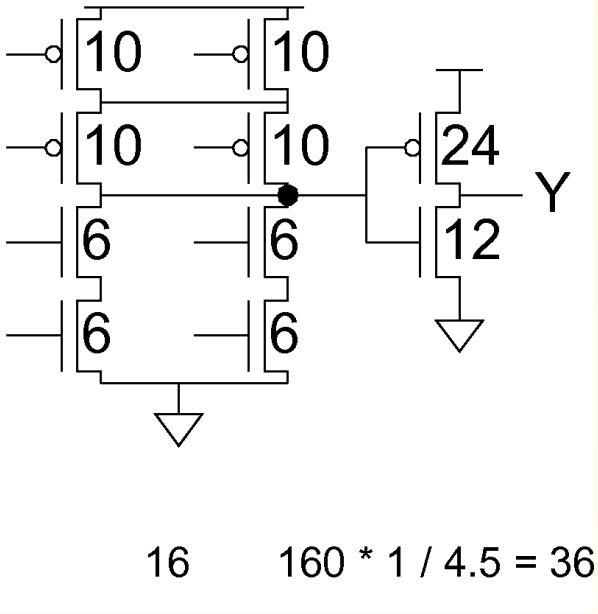


$H = 160/16 = 10$
$B = 1$
$N = 2$
$P = 4 + 1 = 5$
$G = (6/3) \cdot (1) = 2$
$F = GBH = 20$
$\hat{f} = \sqrt[N]{F} = 4.5$
$D = N\hat{f} + P = 14\tau$

Example, Cont'd

Annotate the designs for the multiplexer with transistor sizes which achieve the minimum delay

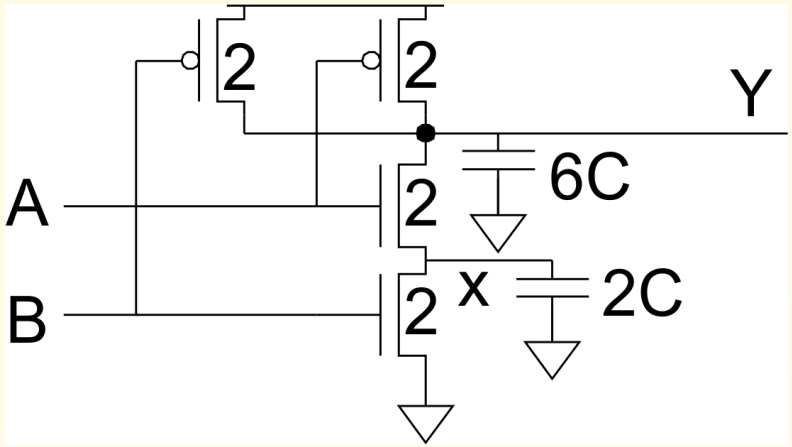




Order of Inputs to a Transistor Stack

Delay of CMOS gate is affected by input order

- Parasitic delay model used in logical effort calculations is too simple
- Example, calculate parasitic delay for Y falling
  - If A arrives latest: 2τ
  - If B arrives latest: 2.33τ



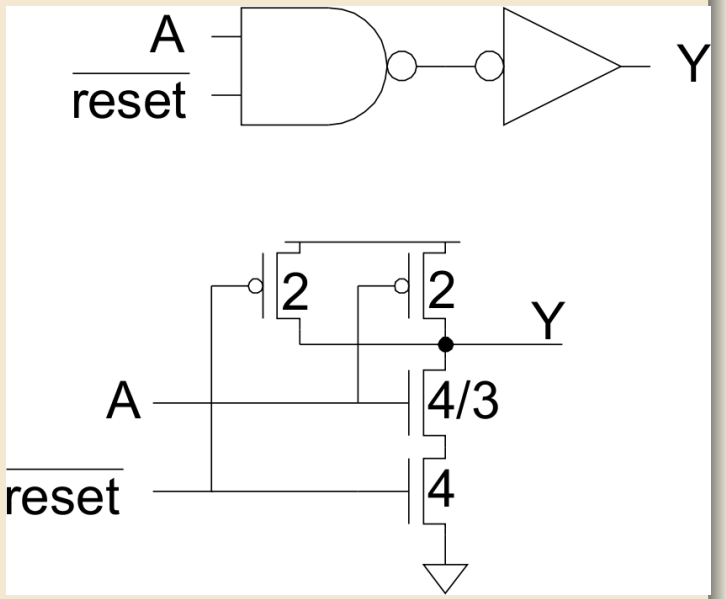
Choosing inner and outer inputs

- **Outer** input is closest to rail (power or ground): **B**
- **Inner** input is closest to output: **A**
- If input arrival time is known
  - **Connect latest arriving input to inner terminal**

Asymmetric Gates

Asymmetric gates favor one input over another

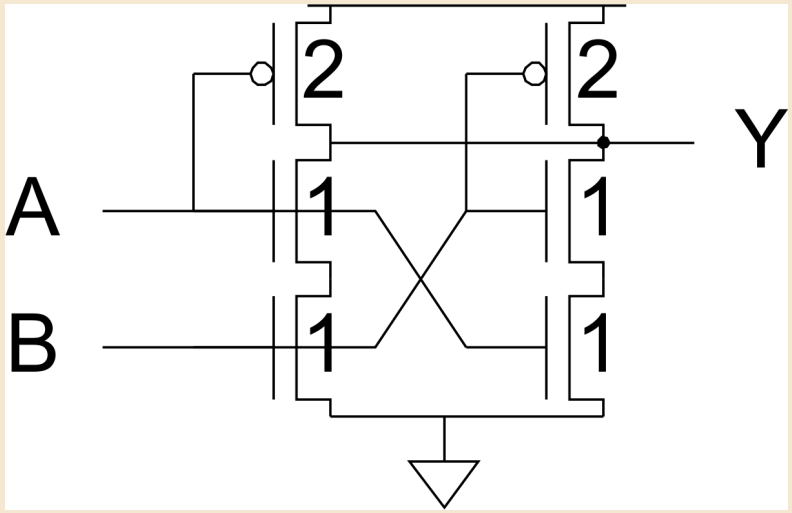
- Example, suppose input A of a NAND gate is most critical
  - Use smaller transistor on A (less capacitance)
  - Boost size of noncritical input
  - So total resistance is same



- Calculate logical effort
  - $g_A = 10/9$
  - $g_B = 2$
  - $g_{total} = g_A + g_B = 28/9$
- Symmetric gate approaches g = 1 on critical input
- However, total logical effort goes up

Symmetric Gates

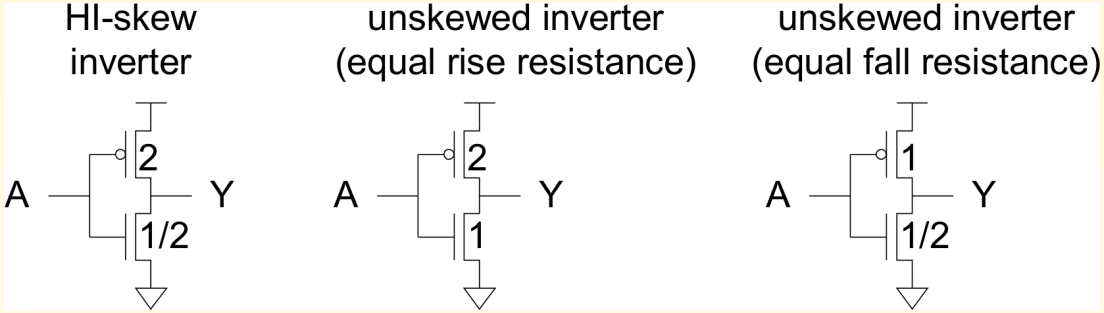
Inputs can be made perfectly symmetric



Make both A and B behave like inner/outer inputs, and keep the P:N ratio 2:1

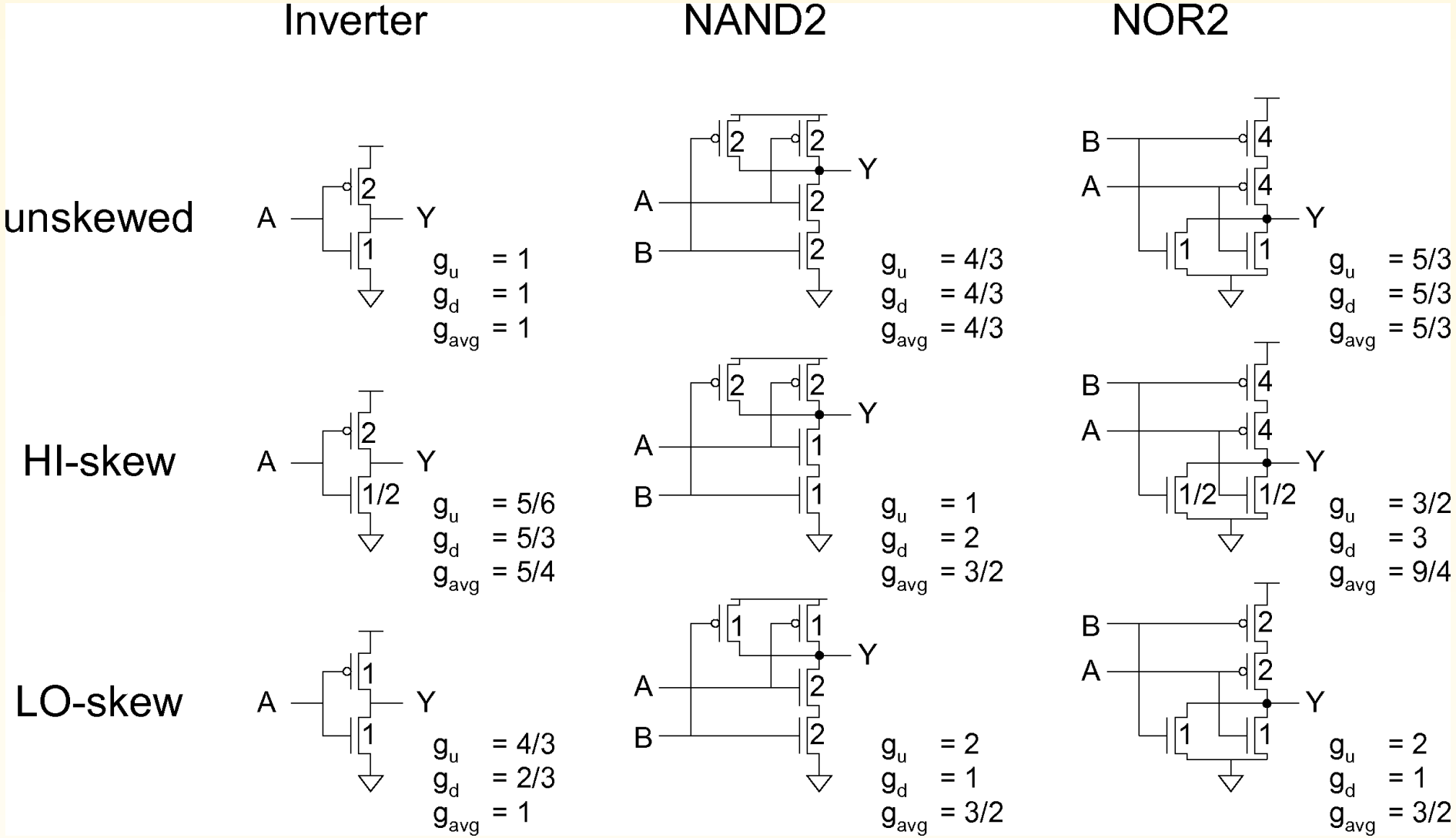
Skewed Gates Favor One Edge Over Another

- Example, suppose rising output of inverter is most critical
  - Downsize noncritical nMOS transistor



- Calculate logical effort by comparing to unskewed inverter with same effective resistance on that edge
  - $g_u = 2.5/3 = 5/6; \quad g_d = 2.5/1.5 = 5/3$
- Definition: Logical effort of a skewed gate for a particular transition is the ratio of the input capacitance of that gate to the input capacitance of an unskewed inverter delivering the same output current for the same transition
- Skewed gates reduce size of noncritical transistors
  - **HI-skew** gates favor **rising output** (small nMOS)
  - **LO-skew** gates favor **falling output** (small pMOS)
- Logical effort is smaller for favored direction, but larger for the other direction

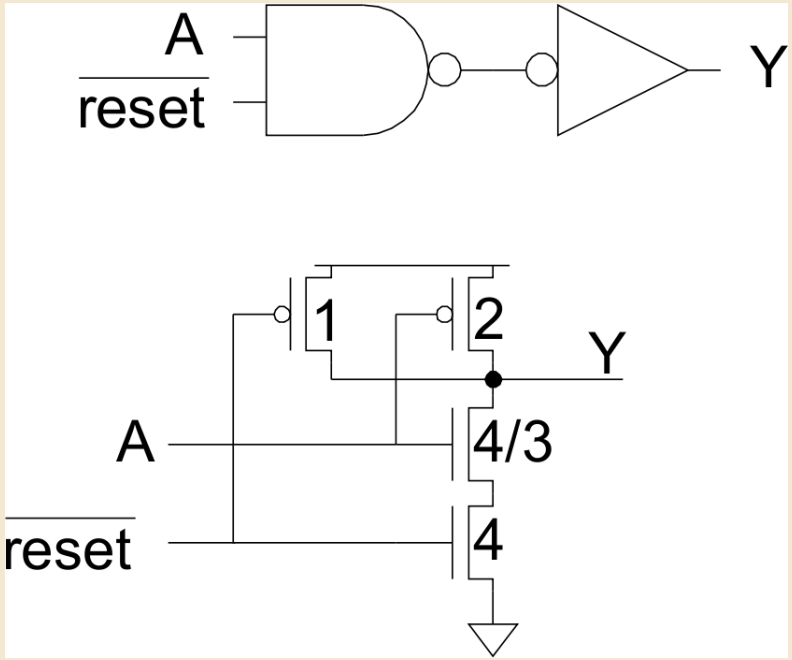
Catalog of Skewed Gates



Asymmetric Skew

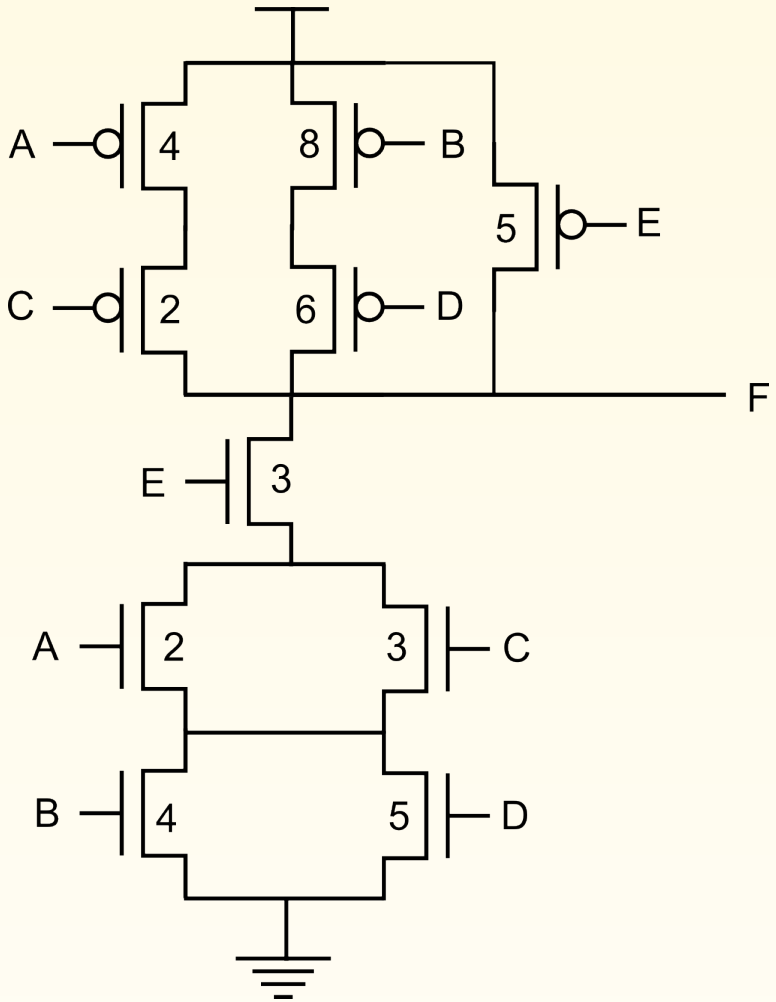
Combine asymmetric and skewed gates

- Downsize noncritical transistor on unimportant input
- Reduces parasitic delay for critical input



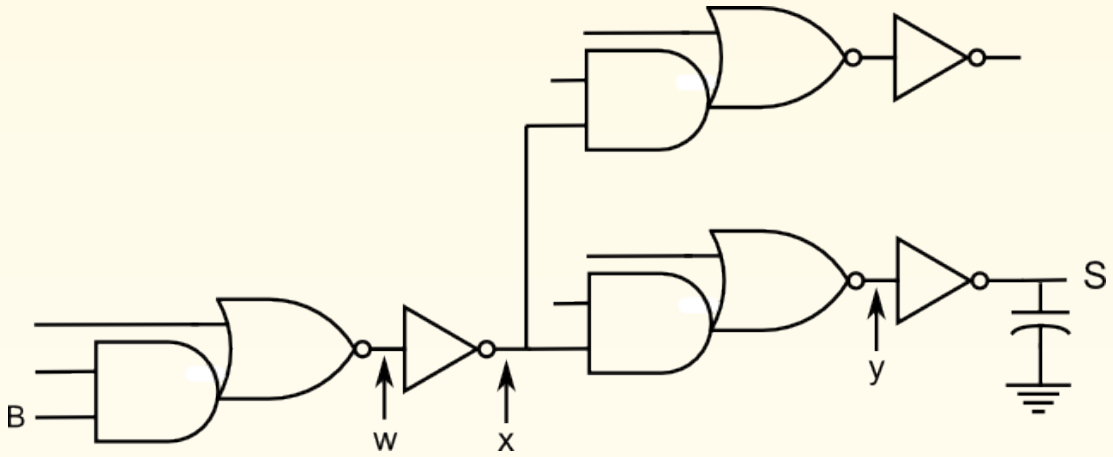
Example – I

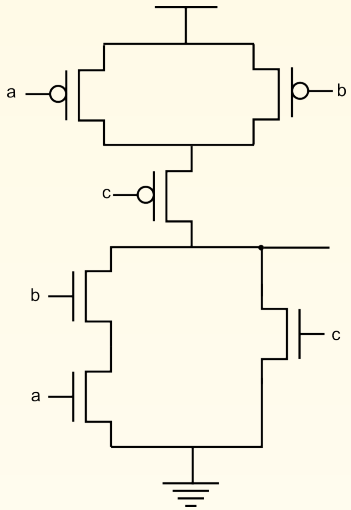
Find the (worst case) logical efforts of the different inputs in the CMOS circuit below.



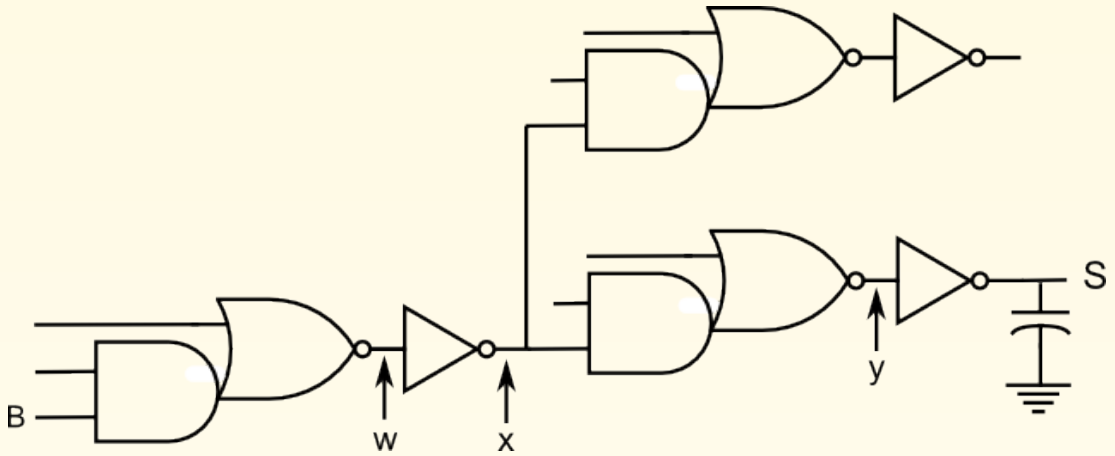
Example - II

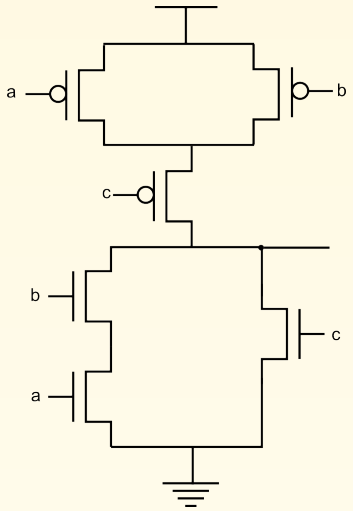
(a) Calculate the delay of the segment from B to S of the adder shown below (the AOI21 is a single stage, shown on the right), given that the output capacitance is 25 units (normalized), and the input capacitance at B is 6 units.





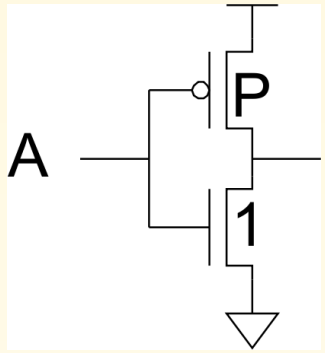
Example - II, Cont'd





(b) Calculate the capacitances of the nodes y, x and w, and the resulting widths of the transistors.

Best P/N Ratio



- We have selected P/N ratio for unit rise and fall resistance (μ = 2-3 for an inverter).
- Alternative: choose ratio for least average delay
  - Example: inverter
    - Delay driving identical inverter
    - $t_{pdf} = (P + 1)$
    - $t_{pdr} = (P + 1)(\mu/P)$
    - $t_{pd} = (P + 1)(1 + \mu/P)/2 = (P + 1 + \mu + \mu/P)/2$
    - Differentiating t_{pd} w.r.t. P, we get, least delay for $P = \sqrt{\mu}$
  - In general, best P/N ratio is sqrt of that giving equal delay
    - Only improves average delay slightly for inverters
    - But significantly decreases area and power