Ye Wang

PhD Candidate

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Objective

- Full-time R&D position in EDA

Education

- **PhD: The University of Texas at Austin** — Austin, TX
  Electrical and Computer Engineering — Aug. 2012 – May. 2018
  - PhD Thesis: Novel Convex Optimization Techniques for Circuit Analysis and Synthesis
  - Advisors: Prof. Michael Orshansky, Prof. Constantine Caramanis
  - GPA: 3.93/4.0
  - Related Courses: Large-Scale Optimization, Nanometer Scale IC Design, VLSI II, Combinatorics & Graph Theory, Numerical Analysis: Linear Algebra, Engineering Programming Language, Advanced Algorithm, Probability & Stochastic Process I, Advanced Probability, High Speed Arithmetic, Mixed-Signal System Design & Modeling, Data Converters, Analog IC Design
- **BEng: Zhejiang University** — Hangzhou, China
  Electronic and Information Engineering — Sept. 2008 – Jun. 2012
  - Advisors: Prof. Yun Pan, Prof. Xiaolang Yan
  - Overall GPA: 3.91/4.0 Major GPA: 3.99/4.0 Rank: 1 (among 112)

Expertise

- **EDA:** modeling and optimization of analog circuits, power grid analysis and simulation
- **Machine learning:** convex optimization, deep learning, hardware acceleration of learning algorithms
- **Hardware security:** PUF-based key generation, lattice-based cryptography

Awards

- George J. Heuer, Jr. Ph.D. Endowed Graduate Fellowship, University of Texas at Austin 2017
- DAC PhD Forum Scholarship, Design Automation Conference 2015
- TI Outstanding Student Designer Award: First Place, University of Texas at Austin 2013

Publications

1. **Y. Wang** and M. Orshansky. "Efficient Helper Data Reduction in SRAM PUFs via Lossy Compression," Under review of *Design, Automation and Test in Europe (DATE)*, 2018
2. A. Aysu, **Y. Wang**, P. Schaumont, and M. Orshansky. "A New Maskless Debiasing Method for Lightweight Physical Unclonable Functions," In *International Symposium on Hardware Oriented Security and Trust (HOST)*, 2017
3. **Y. Wang**, C. Caramanis, and M. Orshansky. "Exploiting Randomness in Sketching for Efficient Hardware Implementation of Machine Learning Applications," In *International Conference on Computer-Aided Design (ICCAD)*, 2016
4. M. Li, **Y. Wang**, and M. Orshansky. "A Monte Carlo Simulation Flow for SEU Analysis of Sequential Circuits," In *Design Automation Conference (DAC)*, 2016
5. **Y. Wang**, C. Caramanis, and M. Orshansky. "PolyGP:Improving GP-Based Analog Optimization through Accurate High-Order Monomials and Semidefinite Relaxation," In *Design, Automation and Test in Europe (DATE)*, 2016
6. **Y. Wang**, C. Caramanis, and M. Orshansky. "PolyGP:Improving GP-Based Analog Optimization through Accurate High-Order Monomials and Semidefinite Relaxation," In *International Workshop on Frontiers in Analog CAD (FAC)*, 2015

7. **Y. Wang**, M. Li, X. Yi, Z. Song, M. Orshansky, and C. Caramanis. "A Novel Power Grid Reduction Method Based on L1 Regularization," In *Design Automation Conference (DAC)*, 2015
8. **Y. Wang**, C. Caramanis, and M. Orshansky. "Enabling Efficient Analog Synthesis by Coupling Sparse Regression and Polynomial Optimization," In *Design Automation Conference (DAC)*, 2014
9. **Y. Wang** and M. Orshansky. "Reducing Amount of Helper Data in Cryptographic Key Generators Based on Physical Unclonable Functions," *US patent pending*
10. **Y. Wang** and M. Orshansky. "Estimating Bit Error Rate of Physical Unclonable Function Under Environmental Variations Using High-Dimensional Stochastic Modeling," *US patent pending*

Research Experience

- PUF-based Key Generation and Optimization — Spring 2016 – Fall 2017
  - Development of a lossy compression algorithm to reduce OTP bits (fuses) by 2.5X in SRAM PUFs
  - System implementation on both FPGA and NIOS II softcore
  - Related tools: Quartus (Verilog), NIOS EDS (C)
- Hardware Acceleration of Machine Learning Algorithms — Spring 2014 – present
  - Implementation of a hardware-efficient random projection algorithm for classification and PCA
  - Applying the random projection to convolutions in deep neural networks to save energy
  - System implementation on FPGA
  - Related tools: Tensorflow (Python), Xilinx Vivado (Verilog), Xilinx Vivado HLS (C)
- Equation-based Analog Circuit Sizing — Fall 2012 – Spring 2014
  - Analog circuit modeling via sparse polynomial for improved accuracy and efficient optimization
  - Introduction of semidefinite relaxation for solving non-convex analog optimization problems
  - Related tools: HSPICE, MATLAB

Industrial Experience

- Samsung Austin R&D Center, Austin, TX, Summer Intern — May. 2014 – Aug. 2014
  - Development of a fast linear solver for power grid analysis
  - Standard cell library characterization for gate sizing
  - Related tools: HSPICE, C++
- Broadcom, Santa Clara, CA, Summer Intern — May. 2013 – Aug. 2013
  - Development of accurate and compact delay model for silicon characterization
  - Conduction of silicon measurement to validate the constructed delay model
  - Related tools: HSPICE, Python

Skills

- **Languages:** C/C++, Verilog, Python, Tcl, SPICE, Assembly, LaTeX
- **Applications:** Cadence tools (Virtuoso, Spectre, Encounter), Synopsys tools (HSPICE, DC, ICC, PT), GNU tools (gcc/g++, gdb), Modelsim, Vivado, Quartus, MATLAB, Vim
- **Operating Systems:** Linux/Unix, Windows
- **Deep Learning Frameworks:** Caffe, Tensorflow

Employability Status: F-1 Student Visa